SYC SEMICONDUCTORES Y COMPONENTES

CD4089

CMOS Binary Rate Multiplier

Features

- **High Voltage Type (20V Rating)**
- **Cascadable in Multiples of 4 Bits**
- **Set to “15” Input and “15” Detect Output**
- **100% Tested for Quiescent Current at 20V**
- **5V, 10V and 15V Parametric Ratings**
- **Standardized Symmetrical Output Characteristics**
- **Maximum Input Current of 1µA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C**
- **Noise Margin (Over Full Package/Temperature Range)**
  - **1V at VDD = 5V**
  - **2V at VDD = 10V**
  - **2.5V at VDD = 15V**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, “Standard Specifications for Description of ‘B’ Series CMOS Devices”**

Applications

- **Numerical Control**
- **Instrumentation**
- **Digital Filtering**
- **Frequency Synthesis**

Description

CD4089BMS is a low power 4 bit digital rate multiplier that provides an output pulse rate that is the clock-input-pulse rate multiplied by $^{1}/_{16}$ times the binary input. For example, when the binary input number is 13, there will be 13 output pulses for every 16 input pulses. This device may be used in conjunction with an up/down counter and control logic used to perform arithmetic operations (adds, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigometric functions, A/D and D/A conversions, and frequency division.

For words of more than 4 bits, CD4089BMS devices may be cascaded in two different modes: an Add mode and a Multiply mode (see Figures 3 and 4). In the Add mode some of the gaps left by the more significant unit at the count of 15 are filled in by the less significant units. For example, when two units are cascaded in the Add mode and programmed to 11 and 13, respectively, the more significant unit will have 11 output pulses for every 16 input pulses and the other unit will have 13 output pulses for every 256 input pulses for a total of

$$\frac{11}{16} + \frac{13}{256} = \frac{189}{256}$$

In the Multiply mode the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second multiplier. Thus the output rate will be

$$\frac{11}{16} \times \frac{13}{16} = \frac{143}{256}$$

The CD4089BMS has an internal synchronous 4 bit counter which, together with one of the four binary input bits, produces pulse trains as shown in Figure 6.

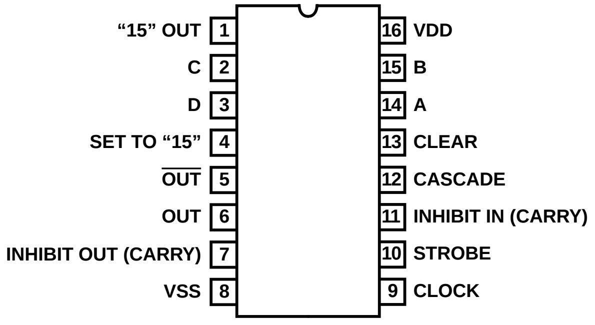
If more than one binary input bit is high, the resulting pulse train is a combination of the separate pulse trains as shown in Figure 6.

The CD4089BMS is supplied in these 16-lead outline packages:

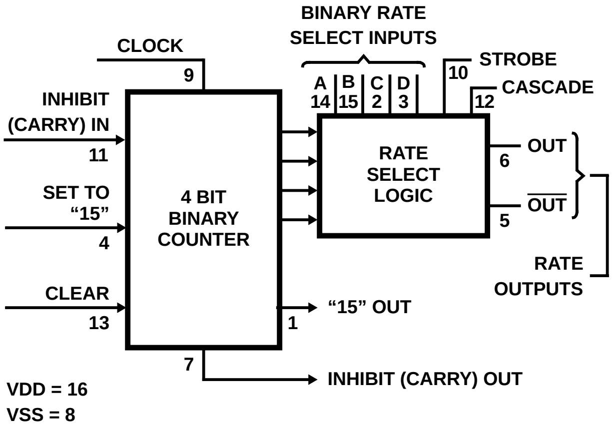
Braze Seal DIP	H4W
Frit Seal DIP	H2R
Ceramic Flatpack	H6P

Pinout

CD4089BMS
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . .-0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . ±10mA
Operating Temperature Range. . . . . -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) . . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25^{o}C	-	300	ns
			10, 11	+125^{o}C, -55^{o}C	-	405	ns
Propagation Delay Clear to Out	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25^{o}C	-	760	ns
			10, 11	+125^{o}C, -55^{o}C	-	1026	ns
Propagation Delay Cascade to Out	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25^{o}C	-	180	ns
			10, 11	+125^{o}C, -55^{o}C	-	243	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25^{o}C	-	200	ns
			10, 11	+125^{o}C, -55^{o}C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25^{o}C	1.2	-	MHz
			10, 11	+125^{o}C, -55^{o}C	.89	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55^{o}C and +125^{o}C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55^{o}C, +25^{o}C	-	5	µA
				+125^{o}C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55^{o}C, +25^{o}C	-	10	µA
				+125^{o}C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55^{o}C, +25^{o}C	-	10	µA
				+125^{o}C	-	600	µA
Output Voltage	VOL5	VDD = 5V, No Load	1, 2	+25^{o}C, +125^{o}C, -55^{o}C	-	50	mV
Output Voltage	VOL10	VDD = 10V, No Load	1, 2	+25^{o}C, +125^{o}C, -55^{o}C	-	50	mV
Output Voltage	VOH5	VDD = 5V, No Load	1, 2	+25^{o}C, +125^{o}C, -55^{o}C	4.95	-	V
Output Voltage	VOH10	VDD = 10V, No Load	1, 2	+25^{o}C, +125^{o}C, -55^{o}C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125^{o}C	0.36	-	mA
				-55^{o}C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125^{o}C	0.9	-	mA
				-55^{o}C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125^{o}C	2.4	-	mA
				-55^{o}C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125^{o}C	-	-0.36	mA
				-55^{o}C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125^{o}C	-	-1.15	mA
				-55^{o}C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125^{o}C	-	-0.9	mA
				-55^{o}C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125^{o}C	-	-2.4	mA
				-55^{o}C	-	-4.2	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25^{o}C, +125^{o}C, -55^{o}C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25^{o}C, +125^{o}C, -55^{o}C	+7	-	V
Propagation Delay Clock to $\overline{\text{Out}}$	TPHL4 TPLH4	VDD = 5V	1, 2, 3	+25^{o}C	-	220	ns
		VDD = 10V	1, 2, 3	+25^{o}C	-	110	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	90	ns
Propagation Delay Clock to Out	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25^{o}C	-	150	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	120	ns
Propagation Delay Clock to Inhibit Out	TPHL5	VDD = 5V	1, 2, 3	+25^{o}C	-	720	ns
		VDD = 10V	1, 2, 3	+25^{o}C	-	320	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	220	ns
Propagation Delay Clock to Inhibit Out	TPLH5	VDD = 5V	1, 2, 3	+25^{o}C	-	500	ns
		VDD = 10V	1, 2, 3	+25^{o}C	-	200	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	150	ns
Propagation Delay Clear to Out	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25^{o}C	-	350	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	260	ns
Propagation Delay Cascade to Out	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25^{o}C	-	90	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	70	ns
Propagation Delay Clock to “9” or “15” Out	TPHL6 TPLH6	VDD = 5V	1, 2, 3	+25^{o}C	-	600	ns
		VDD = 10V	1, 2, 3	+25^{o}C	-	250	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	180	ns
Propagation Delay Inhibit In to Inhibit Out	TPHL7 TPLH7	VDD = 5V	1, 2, 3	+25^{o}C	-	320	ns
		VDD = 10V	1, 2, 3	+25^{o}C	-	150	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	110	ns
Propagation Delay Set to Out	TPHL8 TPLH8	VDD = 5V	1, 2, 3	+25^{o}C	-	660	ns
		VDD = 10V	1, 2, 3	+25^{o}C	-	300	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	220	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25^{o}C	-	100	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25^{o}C	2.5	-	MHz
		VDD = 15V	1, 2, 3	+25^{o}C	3.5	-	MHz
Minimum Inhibit-In Setup Time	TSU	VDD = 5V	1, 2, 3	+25^{o}C	-	100	ns
		VDD = 10V	1, 2, 3	+25^{o}C	-	40	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	20	ns
Minimum Inhibit-In Removal Time	TREM	VDD = 5V	1, 2, 3	+25^{o}C	-	240	ns
		VDD = 10V	1, 2, 3	+25^{o}C	-	130	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	110	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25^{o}C	-	330	ns
		VDD = 10V	1, 2, 3	+25^{o}C	-	170	ns
		VDD = 15V	1, 2, 3	+25^{o}C	-	100	ns
Maximum Clock Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 4	+25^{o}C	-	15	µs
		VDD = 10V	1, 2, 3, 4	+25^{o}C	-	15	µs
		VDD = 15V	1, 2, 3, 4	+25^{o}C	-	15	µs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Minimum Set Removal Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	150	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Clear Removal Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	60	ns
		VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Minimum Set or Clear Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	160	ns
		VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES:
1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

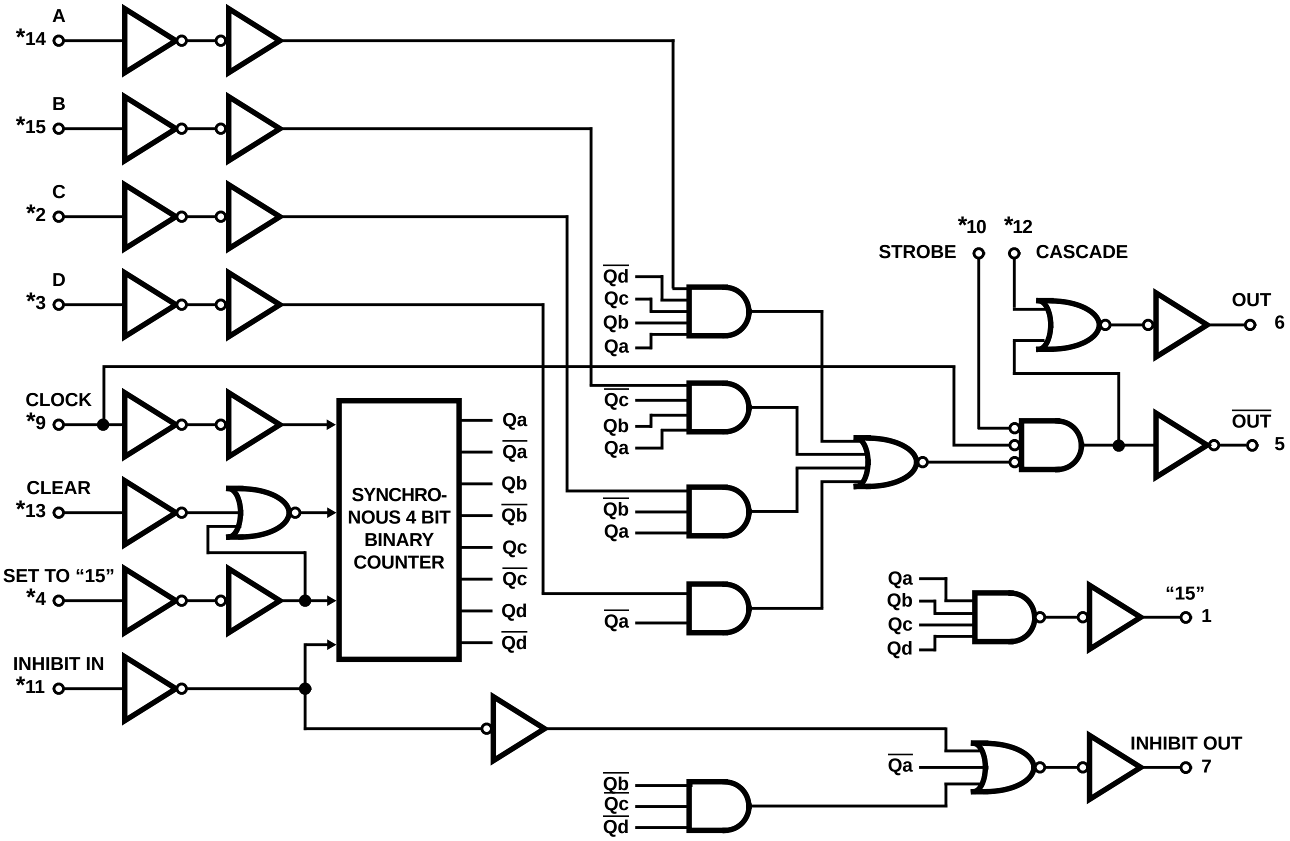
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

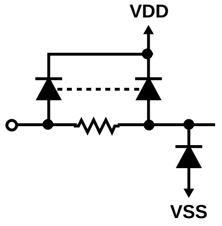
FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	1, 5-7	2-4, 8-15	16			
Static Burn-In 2 (Note 1)	1, 5-7	8	2-4, 9-16			
Dynamic Burn-In (Note 1)	-	2, 4, 8, 10, 12-15	3, 16	1, 5-7	9	11
Irradiation (Note 2)	1, 5-7	8	2-4, 9-16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram





*ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

FIGURE 1. LOGIC DIAGRAM

TRUTH TABLE

INPUTS										OUTPUTS			
NUMBER OF PULSES OR INPUT LOGIC LEVEL (0 = Low; 1 = High; X = Don't Care)										NUMBER OF PULSES OR OUTPUT LOGIC LEVEL (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR	SET	OUT	$\overline{\text{OUT}}$	INH OUT	"15" OUT
0	0	0	0	16	0	0	0	0	0	L	H	1	1
0	0	0	1	16	0	0	0	0	0	1	1	1	1
0	0	1	0	16	0	0	0	0	0	2	2	1	1
0	0	1	1	16	0	0	0	0	0	3	3	1	1
0	1	0	0	16	0	0	0	0	0	4	4	1	1
0	1	0	1	16	0	0	0	0	0	5	5	1	1
0	1	1	0	16	0	0	0	0	0	6	6	1	1
0	1	1	1	16	0	0	0	0	0	7	7	1	1
1	0	0	0	16	0	0	0	0	0	8	8	1	1
1	0	0	1	16	0	0	0	0	0	9	9	1	1
1	0	1	0	16	0	0	0	0	0	10	10	1	1
1	0	1	1	16	0	0	0	0	0	11	11	1	1
1	1	0	0	16	0	0	0	0	0	12	12	1	1
1	1	0	1	16	0	0	0	0	0	13	13	1	1
1	1	1	0	16	0	0	0	0	0	14	14	1	1
1	1	1	1	16	0	0	0	0	0	15	15	1	1
X	X	X	X	16	1	0	0	0	0	**	**	H	**
X	X	X	X	16	0	1	0	0	0	L	H	1	1
X	X	X	X	16	0	0	1	0	0	H	*	1	1
1	X	X	X	16	0	0	0	1	0	16	16	H	L
0	X	X	X	16	0	0	0	1	0	L	H	H	L
X	X	X	X	16	0	0	0	X	1	L	H	L	H

* Output same as the first 16 lines of this truth table (depending on values A, B, C, D)

** Depends on internal state of counter

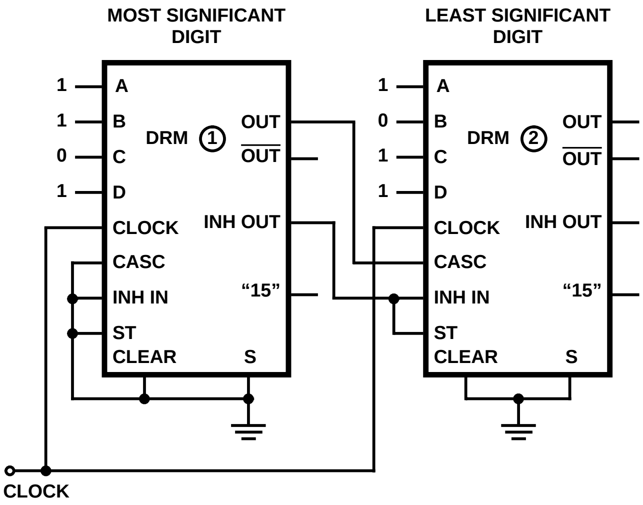


FIGURE 2. TWO CD4089BMS's CASCADED IN THE "ADD" MODE WITH A PRESET NUMBER

OF 189 $\left(\frac{11}{16} + \frac{13}{256} = \frac{189}{256}\right)$

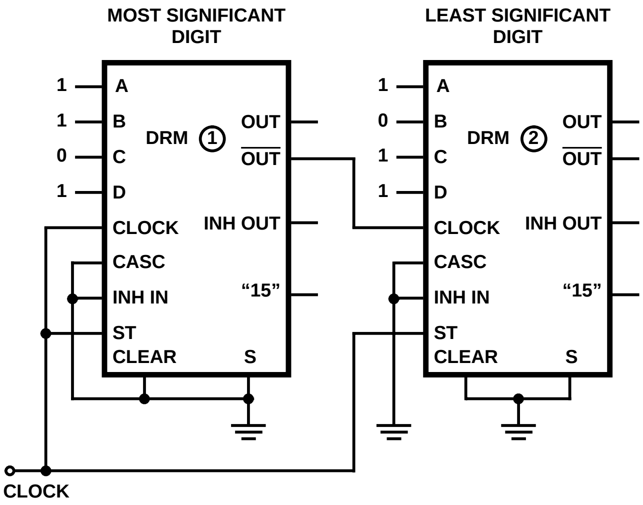
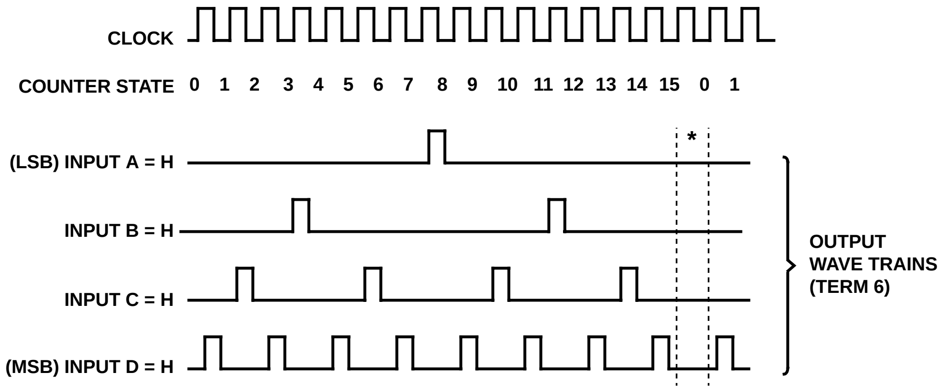


FIGURE 3. TWO CD4089BMS's CASCADED IN THE "MULTIPLY" MODE WITH A PRESET NUMBER

OF 143 $\left(\frac{11}{16} + \frac{13}{16} = \frac{143}{256}\right)$



* AN OUTPUT BIT MAY BE FILLED IN THIS COUNTER STATE
BY A LESS SIGNIFICANT CD4089 CASCADED IN THE ADD MODE

FIGURE 4. TIMING DIAGRAM

Typical Performance Characteristics

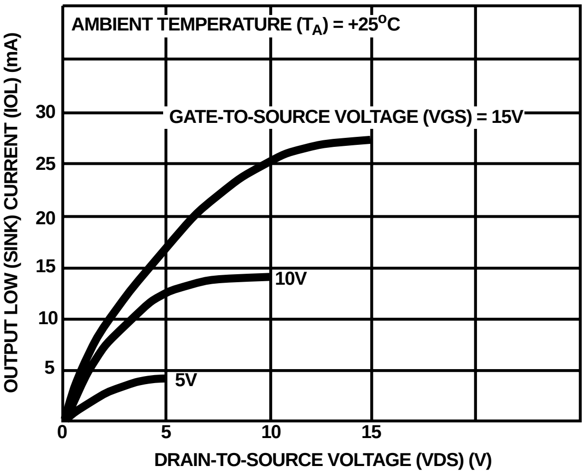


FIGURE 5. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

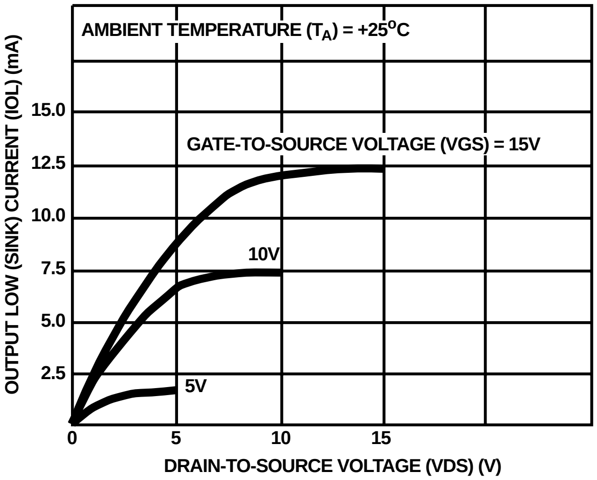


FIGURE 6. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

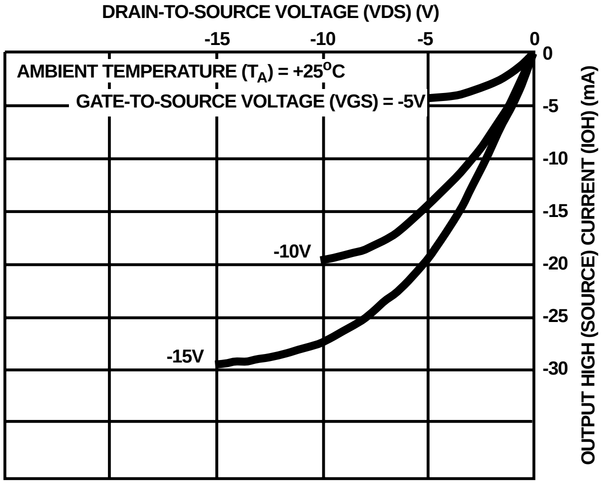


FIGURE 7. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

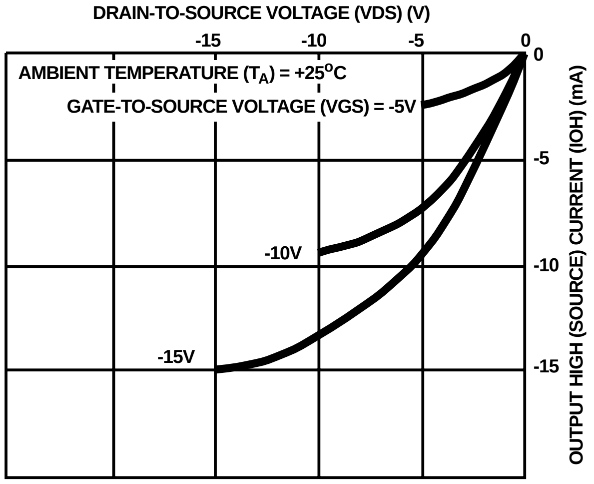


FIGURE 8. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

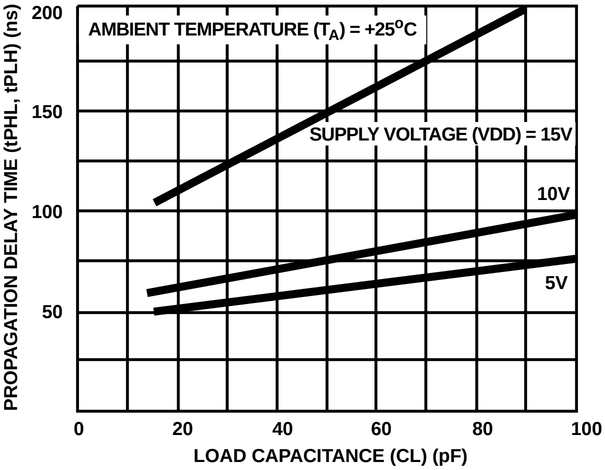


FIGURE 9. TYP. PROPAGATION DELAY TIMES AS FUNCTION OF LOAD CAPACITANCE (CLOCK OR STROBE TO OUT)

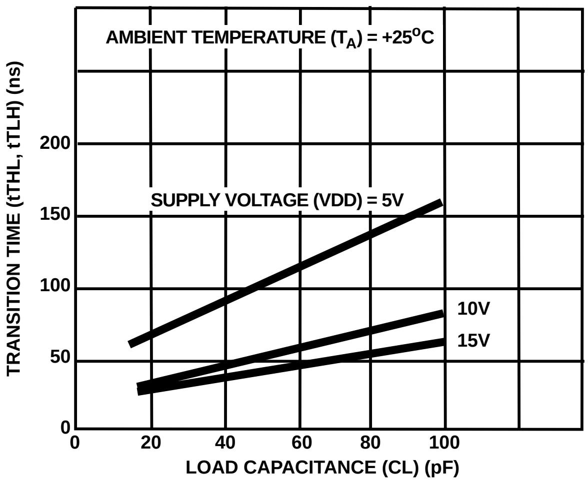


FIGURE 10. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

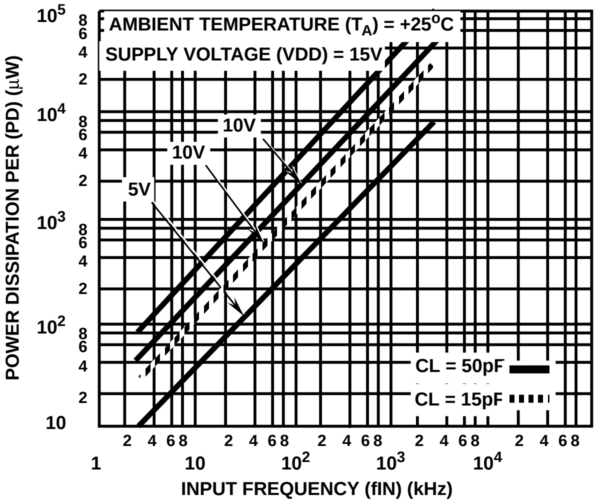
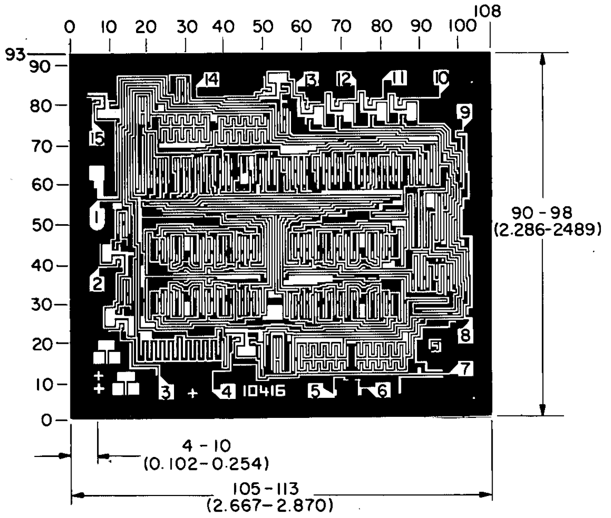


FIGURE 11. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches