OPA134, OPA2134, OPA4134

SBOS058A – DECEMBER 1997 – REVISED OCTOBER 2015

OPAx134 SoundPlus™ High Performance Audio Operational Amplifiers

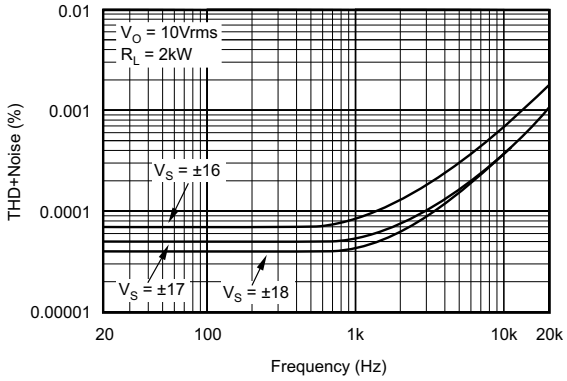
1 Features

- Superior Sound Quality
- Ultra Low Distortion: 0.00008%
- Low Noise: 8 nV/√Hz
- True FET-Input: I_B = 5pA
- High Speed:
  - Slew Rate: 20 V/µs
  - Bandwidth: 8 MHz
- High Open-Loop Gain: 120 dB (600 Ω)
- Wide Supply Range: ±2.5 V to ±18 V
- Single, Dual, and Quad Versions

2 Applications

- Professional Audio and Music
- Line Drivers
- Line Receivers
- Multimedia Audio
- Active Filters
- Preamplifiers
- Integrators
- Crossover Networks

THD+Noise vs Frequency



3 Description

The OPA134 series are ultra-low distortion, low-noise operational amplifiers fully specified for audio applications. A true FET input stage is incorporated to provide superior sound quality and speed for exceptional audio performance. This, in combination with high output drive capability and excellent DC performance, allows for use in a wide variety of demanding applications. In addition, the OPA134 has a wide output swing, to within 1 V of the rails, allowing increased headroom and making it ideal for use in any audio circuit.

The OPA134 SoundPlus™ audio operational amplifiers are easy to use and free from phase-inversion and the overload problems often found in common FET-input operational amplifiers. They can be operated from ±2.5-V to ±18-V power supplies. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over its wide input voltage range, minimizing distortion. OPA134 series operational amplifiers are unity-gain stable and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. The dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Single and dual versions are available in 8-pin DIP and SO-8 surface-mount packages in standard configurations. The quad is available in 14-pin DIP and SO-14 surface mount packages. All are specified for –40°C to 85°C operation. A SPICE macromodel is available for design analysis.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA134	SOIC (8)	3.91 mm × 4.90 mm
	PDIP (8)	6.35 mm × 9.81 mm
OPA2134	SOIC (8)	3.91 mm × 4.90 mm
	PDIP (8)	6.35 mm × 9.81 mm
OPA4134	SOIC (14)	3.91 mm × 8.65 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Electrical Characteristics ... 5
6.5 Typical Characteristics ... 7
7 Detailed Description ... 12
7.1 Overview ... 12
7.2 Functional Block Diagram ... 12
7.3 Feature Description ... 12
7.4 Device Functional Modes ... 14
8 Application and Implementation ... 15
8.1 Application Information ... 15
8.2 Typical Application ... 16
9 Power Supply Recommendations ... 18
10 Layout ... 18
10.1 Layout Guidelines ... 18
10.2 Layout Example ... 19
11 Device and Documentation Support ... 20
11.1 Device Support ... 20
11.2 Documentation Support ... 20
11.3 Related Links ... 20
11.4 Community Resources ... 21
11.5 Trademarks ... 21
11.6 Electrostatic Discharge Caution ... 21
11.7 Glossary ... 21
12 Mechanical, Packaging, and Orderable Information ... 21

4 Revision History

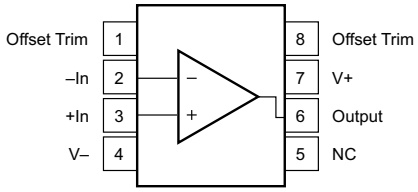
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2000) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

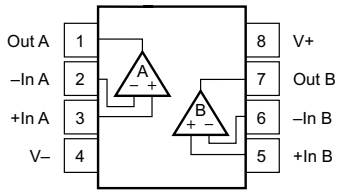
Copyright © 1997–2015, Texas Instruments Incorporated

5 Pin Configuration and Functions

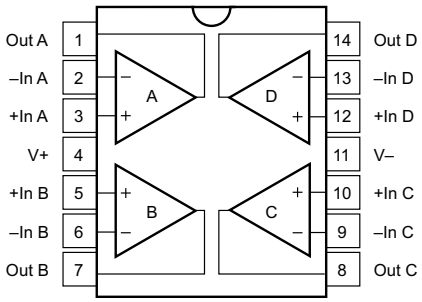
OPA134: P and D Packages
8-Pin PDIP and 8-Pin SOIC
Top View



OPA2134: P and D Packages
8-Pin PDIP and 8-Pin SOIC
Top View



OPA4134: P and D Packages
14-Pin PDIP and 14-Pin SOIC
Top View



Pin Functions: OPA134

PIN		I/O	DESCRIPTION
NAME	NO.		
Offset Trim	1	I	Input offset voltage adjust
–In	2	I	Inverting input
+In	3	I	Noninverting input
V–	4	—	Negative power supply
NC	5	—	No internal connection. Can be left floating.
Output	6	O	Output
V+	7	—	Positive power supply
Offset Trim	8	I	Input offset voltage adjust

Pin Functions: OPA2134 and OPA4134

PIN			I/O	DESCRIPTION
NAME	OPA2134 NO.	OPA4134 NO.		
Out A	1	1	O	Output channel A
–In A	2	2	I	Inverting input channel A
+In A	3	3	I	Noninverting input channel A
V+	8	4	—	Positive power supply
+In B	5	5	I	Noninverting input channel B
–In B	6	6	I	Inverting input channel B
Out B	7	7	O	Output channel B
Out C	—	8	O	Output channel C
–In C	—	9	I	Inverting input channel C
+In C	—	10	I	Noninverting input channel C

Copyright © 1997–2015, Texas Instruments Incorporated

Pin Functions: OPA2134 and OPA4134 (continued)

PIN			I/O	DESCRIPTION
NAME	OPA2134 NO.	OPA4134 NO.		
V–	4	11	—	Negative power supply
+In D	—	12	I	Noninverting input channel D
–In D	—	13	I	Inverting input channel D
Out D	—	14	O	Output channel D

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	Supply voltage, V+ to V–		36	V
	Input voltage	(V–) –0.7	(V+) +0.7	V
	Output short circuit (2)		Continuous	
	Operating temperature	–40	125	°C
	Junction temperature		150	°C
	Lead temperature (soldering, 10 s)		300	°C
T_{stg}	Storage temperature	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
OPA134 in PDIP and SOIC Package, OPA2134 and OPA4134 in PDIP Package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
OPA2134 in SOIC Package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	
OPA4134 in SOIC Package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VS	Supply voltage, VS = (V+) – (V–)	±2.5	±15	±18	V
T_A	Specified temperature	–40		85	°C

Copyright © 1997–2015, Texas Instruments Incorporated

6.4 Electrical Characteristics

At T_A = +25°C, V_S = ±15 V, unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE							
Total Harmonic Distortion + Noise		G = 1, f = 1 kHz, V_O = 3 Vrms	R_L = 2 kΩ		0.00008%		
			R_L = 600 Ω		0.00015%		
Intermodulation Distortion		G = 1, f = 1 kHz, V_O = 1 Vp-p			–98		dB
Headroom(1)		THD < 0.01%, R_L = 2 kΩ , V_S = 18 V			23.6		dBu
FREQUENCY RESPONSE							
Gain-Bandwidth Product					8		MHz
Slew Rate(2)				±15	±20		V/µs
Full Power Bandwidth					1.3		MHz
Settling Time 0.1%		G = 1, 10-V Step, C_L = 100 pF			0.7		µs
Settling Time 0.01%		G = 1, 10-V Step, C_L = 100 pF			1		µs
Overload Recovery Time		(V_{IN}) × (Gain) = V_S			0.5		µs
NOISE							
Input Voltage Noise	Noise Voltage, f = 20 Hz to 20 kHz				1.2		µVrms
	Noise Density, f = 1 kHz				8		nV/√Hz
Current Noise Density, f = 1 kHz					3		fA/√Hz
OFFSET VOLTAGE							
Input Offset Voltage					±0.5	±2	mV
		T_A = –40°C to 85°C			±1	±3(3)	
Input Offset Voltage vs Temperature		T_A = –40°C to 85°C			±2		µV/°C
Input Offset Voltage vs Power Supply (PSRR)		V_S = ±2.5 V to ±18 V		90	106		dB
Channel Seperation (Dual, Quad)		DC, R_L = 2 kΩ			135		dB
		f = 20 kHz, R_L = 2 kΩ			130		
INPUT BIAS CURRENT							
Input Bias Current(4)		V_{CM} = 0 V			5	±100	pA
Input Bias Current vs Temperature(3)					See *Typical Characteristics*	±5	nA
Input Offset Current(4)		V_{CM} = 0 V			±2	±50	pA
INPUT VOLTAGE RANGE							
Common-Mode Voltage Range				(V–)+2.5	13	(V+)–2.5	V
Common-Mode Rejection		V_{CM} = –12.5 V to 12.5 V		86	100		dB
		T_A = –40°C to 85°C			90		
INPUT IMPEDANCE							
Differential					10^{13} || 2		Ω || pF
Common-Mode		V_{CM} = –12.5 V to 12.5 V			10^{13} || 5		Ω || pF
OPEN-LOOP GAIN							
Open-Loop Voltage Gain		R_L = 10 kΩ , V_O = –14.5 V to 13.8 V		104	120		dB
		R_L = 2 kΩ , V_O = –13.8 V to 13.5 V		104	120		
		R_L = 600 Ω , V_O = –12.8 V to 12.5 V		104	120		

(1) dBu = 20*log (Vrms/0.7746) where Vrms is the maximum output voltage for which THD+Noise is less than 0.01%. See THD+Noise text.
(2) Proposed by design.
(3) Proposed by wafer-level test to 95% confidence level.
(4) High-speed test at T_J = 25°C.

Copyright © 1997–2015, Texas Instruments Incorporated

Electrical Characteristics (continued)

At T_A = +25°C, V_S = ±15 V, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT					
Voltage Output	R_L = 10 kΩ	(V–)+0.5		(V+)–1.2	V
	R_L = 2 kΩ	(V–)+1.2		(V+)–1.5	
	R_L = 600 Ω	(V–)+2.2		(V+)–2.5	
Output Current			±35		mA
Output Impedance, Closed-Loop(5)	f = 10 kHz		0.01		Ω
Output Impedance, Open-Loop	f = 10 kHz		10		Ω
Short-Circuit Current			±40		mA
Capacitive Lead Drive (Stable Operation)			See *Typical Characteristics*		
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±2.5		±18	V
Quiescent Current (per amplifier)	I_O = 0		4	5	mA
TEMPERATURE RANGE					
Specified Range		–40		85	°C
Operating Range		–55		125	°C

(5) See Figure 14

Copyright © 1997–2015, Texas Instruments Incorporated

6.5 Typical Characteristics

At T_A = 25°C, V_S = 15 V, R_L = 2 kΩ, unless otherwise noted.

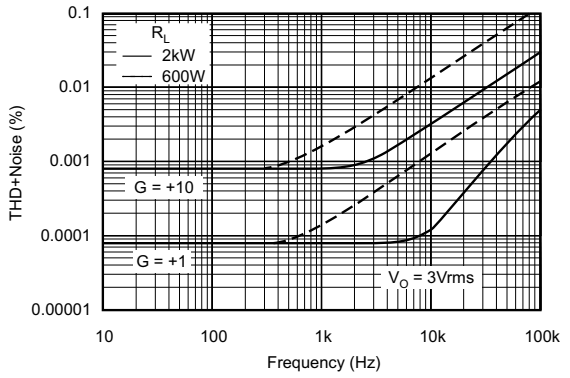


Figure 1. Total Harmonic Distortion + Noise vs Frequency

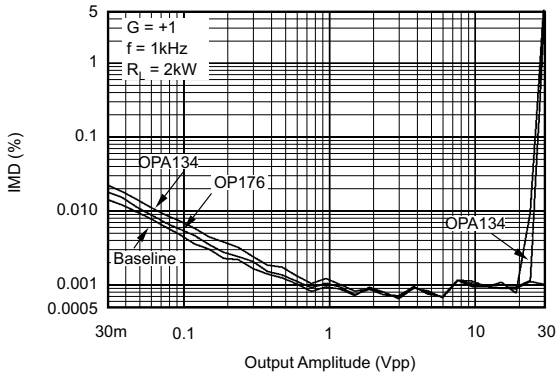


Figure 2. SMPTE Intermodulation Distortion vs Output Amplitude

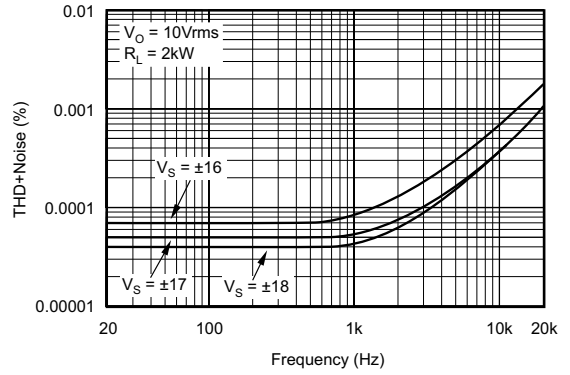


Figure 3. Total Harmonic Distortion + Noise vs Frequency

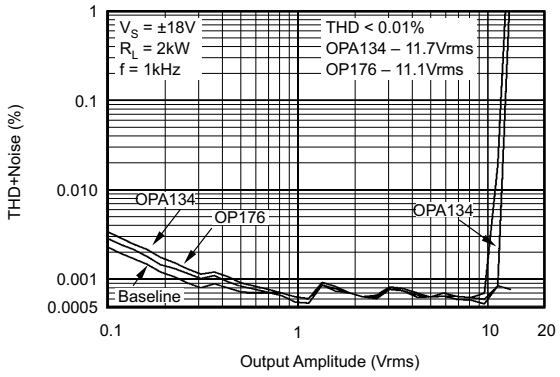


Figure 4. Headroom – Total Harmonic Distortion + Noise vs Output Amplitude

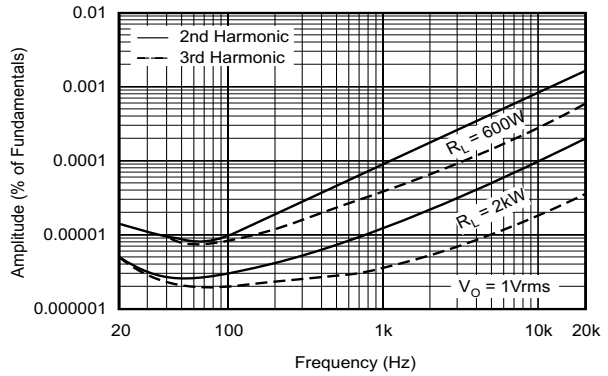


Figure 5. Harmonic Distortion + Noise vs Frequency

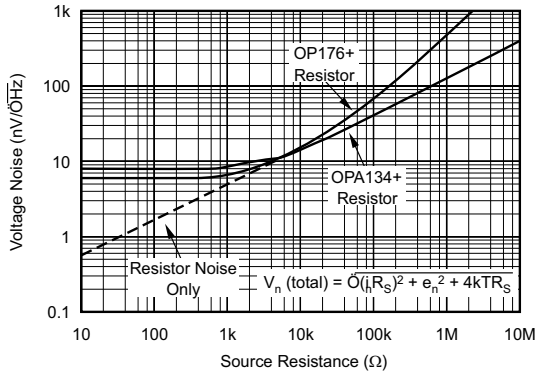


Figure 6. Voltage Noise vs Source Resistance

Copyright © 1997–2015, Texas Instruments Incorporated

Typical Characteristics (continued)

At T_A = 25°C, V_S = 15 V, R_L = 2 kΩ, unless otherwise noted.

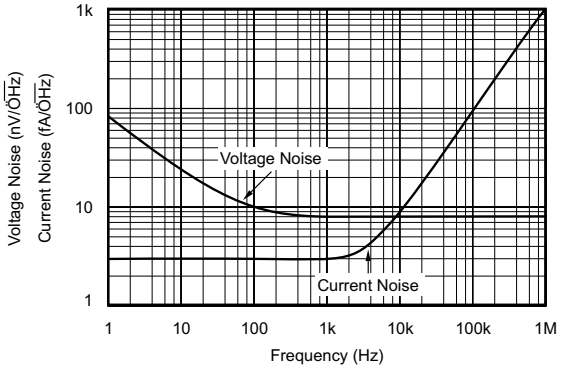


Figure 7. Input Voltage and Current Noise Spectral Density vs Frequency

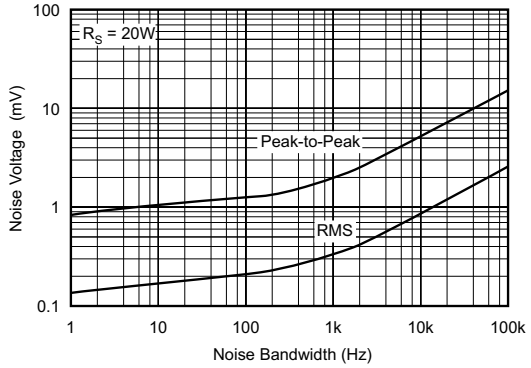


Figure 8. Input-Referred Noise Voltage vs Noise Bandwidth

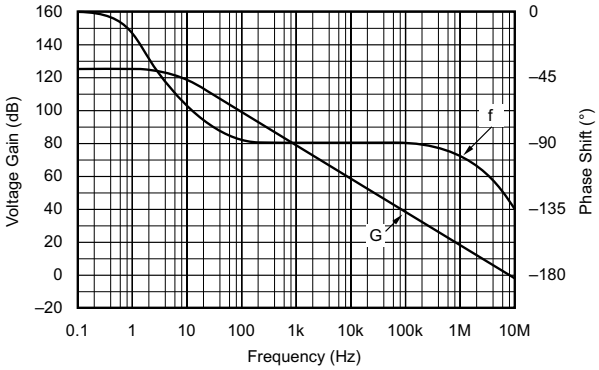


Figure 9. Open-Loop Gain and Phase vs Frequency

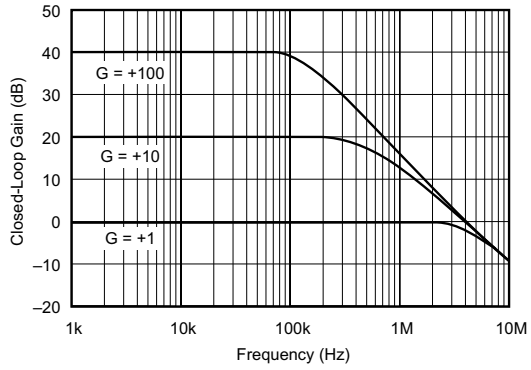


Figure 10. Closed-Loop Gain vs Frequency

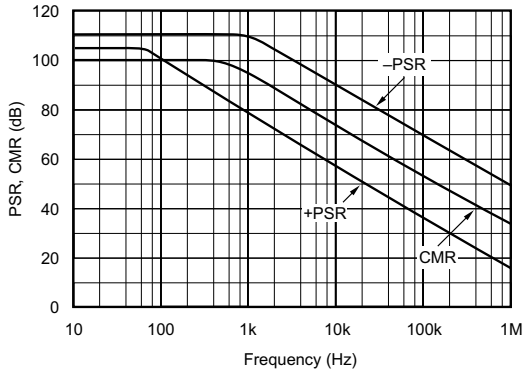


Figure 11. Power Supply and Common-Mode Rejection vs Frequency

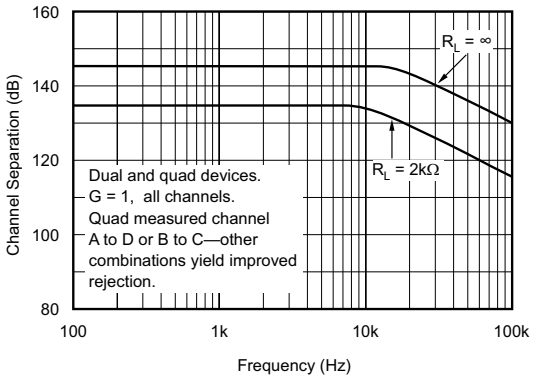


Figure 12. Channel Separation vs Frequency

Copyright © 1997–2015, Texas Instruments Incorporated

Typical Characteristics (continued)

At T_A = 25°C, V_S = 15 V, R_L = 2 kΩ, unless otherwise noted.

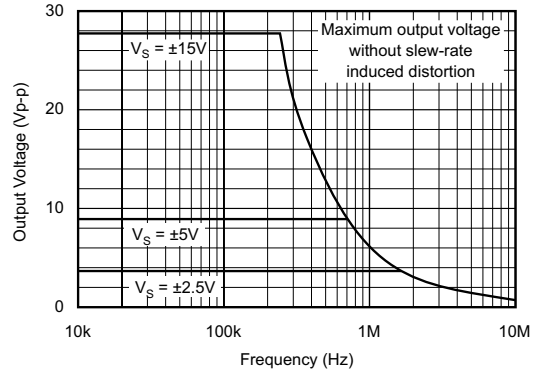


Figure 13. Maximum Output Voltage vs Frequency

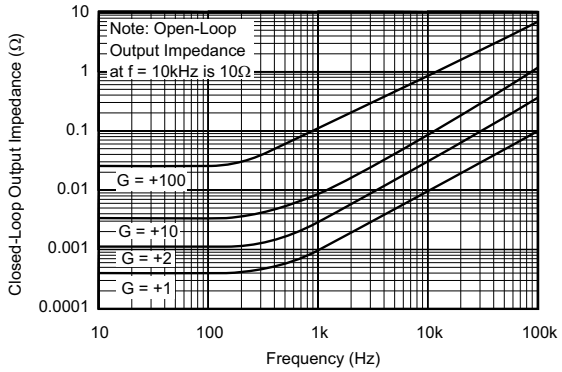


Figure 14. Closed-Loop Output Impedance vs Frequency

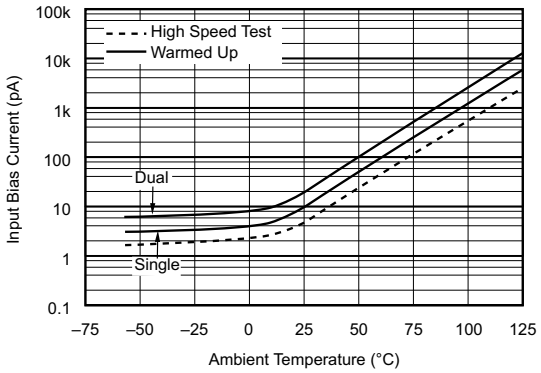


Figure 15. Input Bias Current vs Temperature

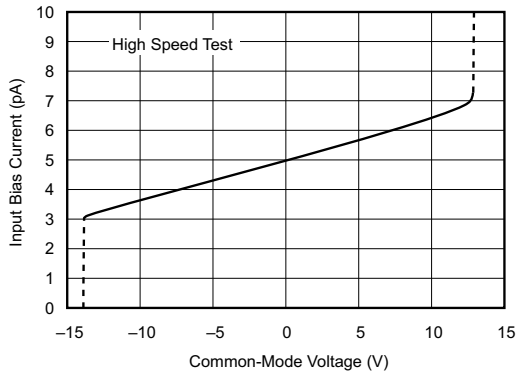


Figure 16. Input Bias Current vs Input Common-Mode Voltage

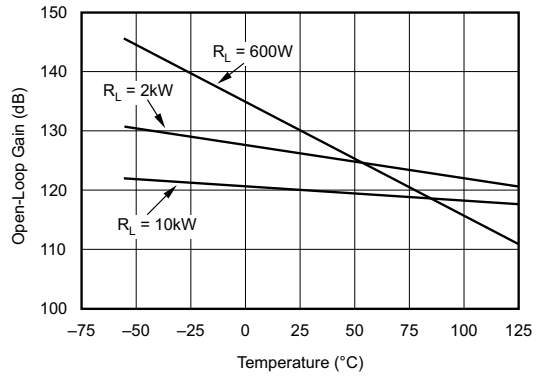


Figure 17. Open-Loop Gain vs Temperature

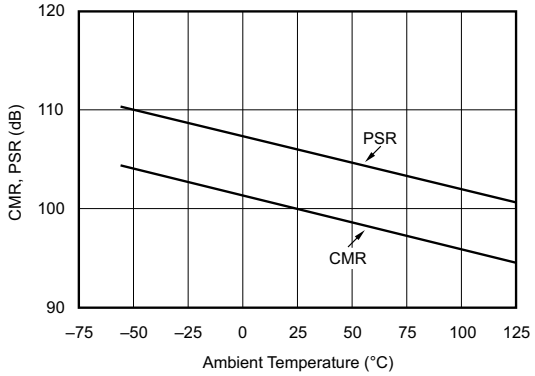


Figure 18. CMR, PSR vs Temperature

Copyright © 1997–2015, Texas Instruments Incorporated

Typical Characteristics (continued)

At T_A = 25°C, V_S = 15 V, R_L = 2 kΩ, unless otherwise noted.

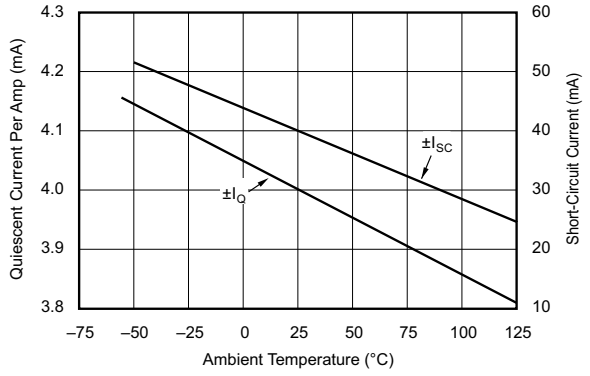


Figure 19. Quiescent Current and Short-Circuit Current vs Temperature

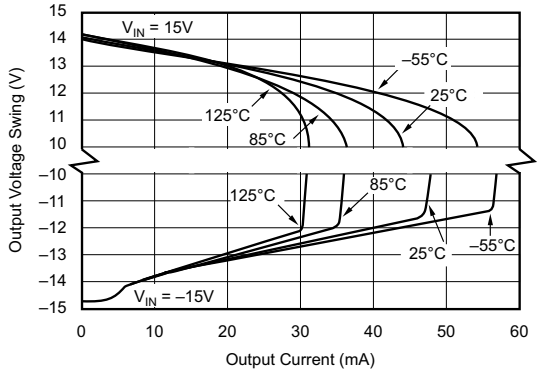


Figure 20. Output Voltage Swing vs Output Current

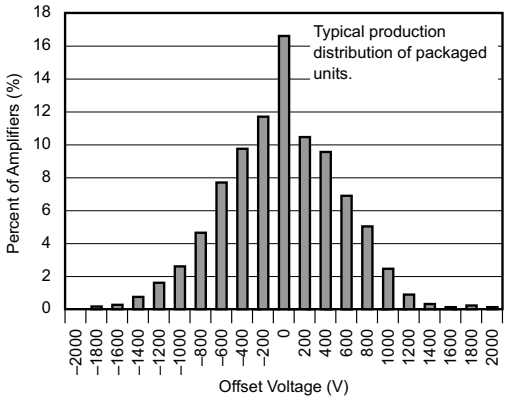


Figure 21. Offset Voltage Production Distribution

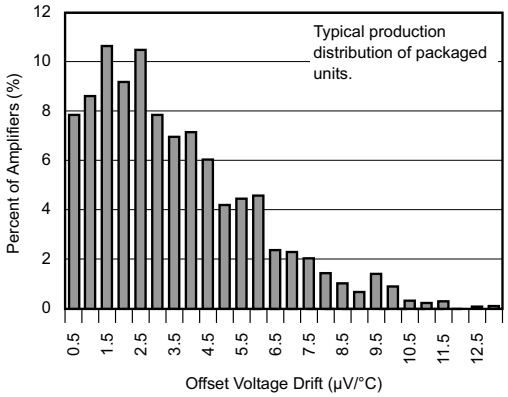


Figure 22. Offset Voltage Drift Production Distribution

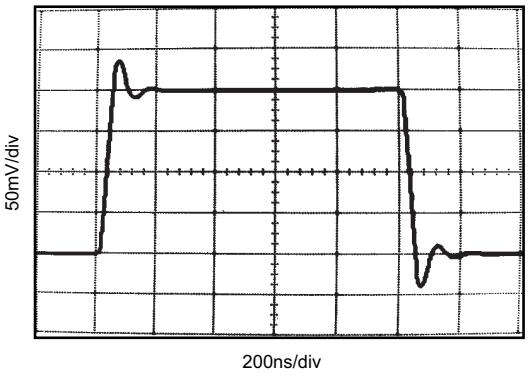


Figure 23. Small-Signal Step Response G = 1, C_L = 100 pF

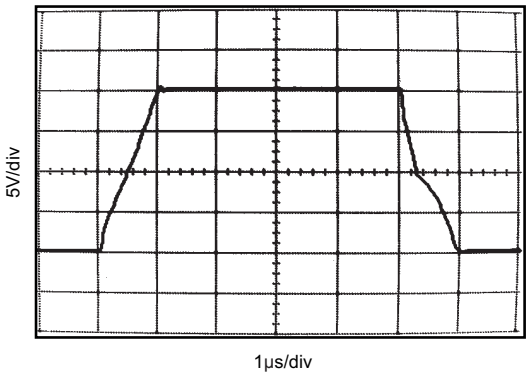


Figure 24. Large-Signal Step Response G = 1, C_L = 100 pF

Copyright © 1997–2015, Texas Instruments Incorporated

Typical Characteristics (continued)

At T_A = 25°C, V_S = 15 V, R_L = 2 kΩ, unless otherwise noted.

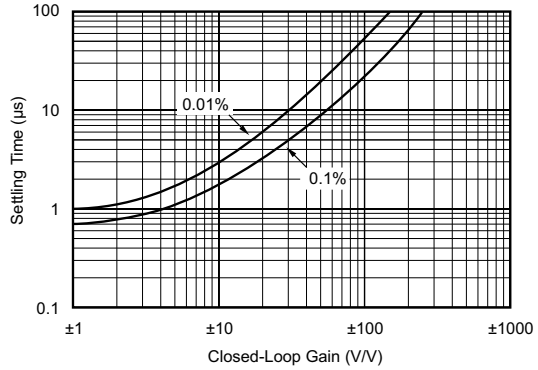


Figure 25. Settling Time vs Closed-Loop Gain

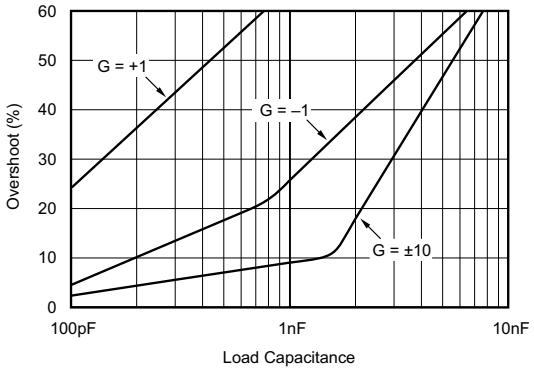


Figure 26. Small-Signal Overshoot vs Load Capacitance

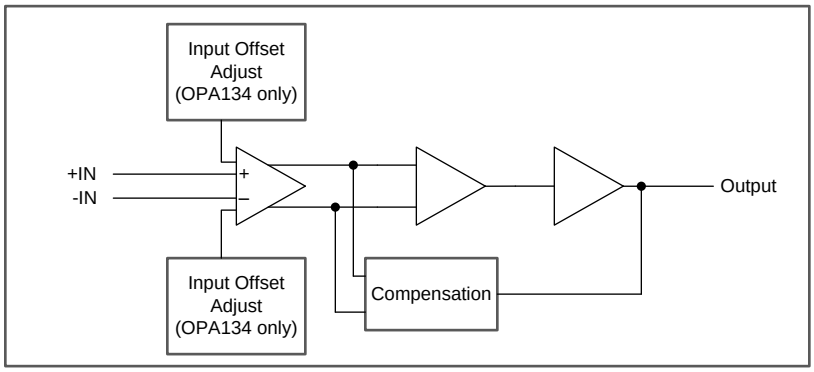
Copyright © 1997–2015, Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The OPA134 series are ultra-low distortion, low-noise operational amplifiers fully specified for audio applications. A true FET input stage is incorporated to provide superior sound quality and speed for exceptional audio performance. This, in combination with high output drive capability and excellent DC performance, allows for use in a wide variety of demanding applications. In addition, the OPA134 has a wide output swing, to within 1 V of the rails, allowing increased headroom and making it ideal for use in any audio circuit.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Total Harmonic Distortion

The OPA134 series of operational amplifiers have excellent distortion characteristics. THD+Noise is below 0.0004% throughout the audio frequency range, 20 Hz to 20 kHz, with a 2-kΩ load. In addition, distortion remains relatively flat through its wide output voltage swing range, providing increased headroom compared to other audio amplifiers, including the OP176/275.

Headroom is a subjective measurement, and can be thought of as the maximum output amplitude allowed while still maintaining a low level of distortion. In an attempt to quantify headroom, TI defines very low distortion as 0.01%. Headroom is expressed as a ratio which compares the maximum allowable output voltage level to a standard output level (1 mW into 600 Ω, or 0.7746 Vrms). Therefore, OPA134 series of operational amplifiers, which have a maximum allowable output voltage level of 11.7 Vrms (THD+Noise < 0.01%), have a headroom specification of 23.6 dBu. See Figure 4.

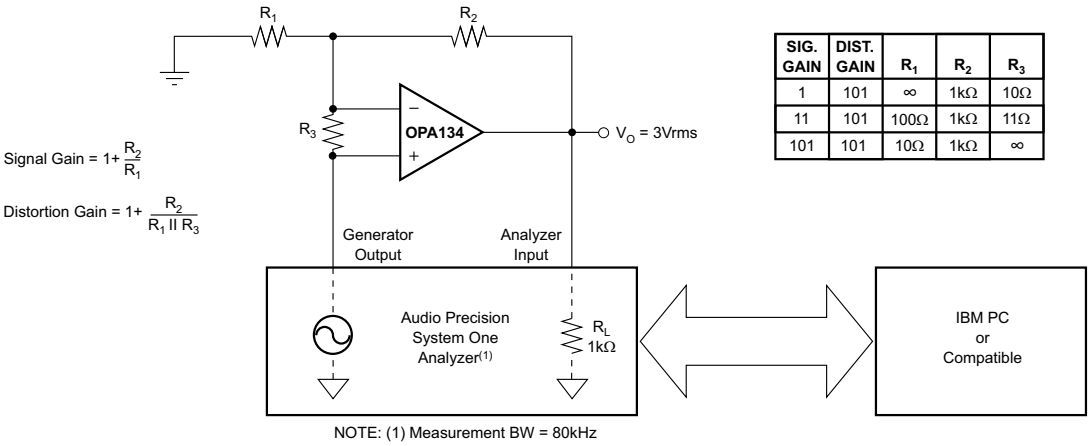
7.3.2 Distortion Measurements

The distortion produced by OPA134 series of operational amplifiers is below the measurement limit of all known commercially-available equipment. However, a special test circuit can extend the measurement capabilities.

Operational amplifier distortion can be considered an internal error source which can be referred to the input. Figure 27 shows a circuit which causes the operational amplifier distortion to be 101 times greater than that which the operational amplifier normally produces. The addition of R3 to the otherwise standard non-inverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. The input signal and load applied to the operational amplifier are the same as with conventional feedback without R3. The value of R3 should be kept small to minimize its effect on the distortion measurements.

Copyright © 1997–2015, Texas Instruments Incorporated

Feature Description (continued)



SIG. GAIN	DIST. GAIN	R_1	R_2	R_3
1	101	∞	1kΩ	10Ω
11	101	100Ω	1kΩ	11Ω
101	101	10Ω	1kΩ	∞

Figure 27. Distortion Test Circuit

This technique can be verified by duplicating measurements at high gain or high frequency, where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision distortion and noise analyzer, which greatly simplifies repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

7.3.3 Source Impedance and Distortion

For lowest distortion with a source or feedback network with an impedance greater than 2 kΩ, the impedance seen by the positive and negative inputs in noninverting applications should be matched. The p-channel JFETs in the FET input stage exhibit a varying input capacitance with applied common-mode input voltage. In inverting configurations, the input does not vary with input voltage, because the inverting input is held at virtual ground. However, in noninverting applications the inputs do vary, and the gate-to-source voltage is not constant. The effect is increased distortion due to the varying capacitance for unmatched source impedances greater than 2 kΩ.

To maintain low distortion, match unbalanced source impedance with the appropriate values in the feedback network as shown in Figure 28. Of course, the unbalanced impedance may be from gain-setting resistors in the feedback path. If the parallel combination of R1 and R2 is greater than 2 kΩ, use a matching impedance on the noninverting input. As always, minimize resistor values to reduce the effects of thermal noise.

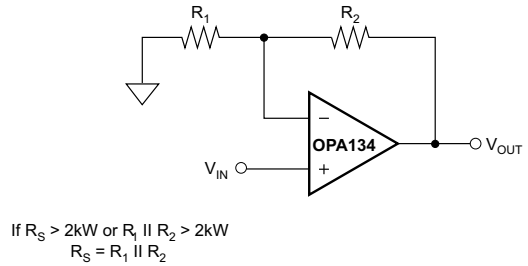


Figure 28. Impedance Matching for Maintaining Low Distortion in Non-Inverting Circuits

7.3.4 Phase Reversal Protection

The OPA134 series of operational amplifiers are free from output phase-reversal problems. Many audio operational amplifiers, such as the OP176, exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. The OPA134 series operational amplifiers are free from this undesirable behavior even with inputs of 10-V beyond the input common-mode range.

Copyright © 1997–2015, Texas Instruments Incorporated

Feature Description (continued)

7.3.5 Output Current Limit

Output current is limited by internal circuitry to approximately ±40 mA at 25°C. The limit current decreases with increasing temperature, as shown in Figure 19.

7.4 Device Functional Modes

7.4.1 Noise Performance

Circuit noise is determined by the thermal noise of external resistors and operational amplifier noise. Operational amplifier noise is described by two parameters: noise voltage and noise current. The total noise is quantified by the equation:

$$V_n(\text{total}) = \sqrt{(i_n R_S)^2 e_n^2 + 4kTR_S} \quad (1)$$

With low source impedance, the current noise term is insignificant and voltage noise dominates the noise performance. At high source impedance, the current noise term becomes the dominant contributor.

Low-noise bipolar operational amplifiers such as the OPA27 and OPA37 provide low voltage noise at the expense of a higher current noise. However, OPA134 series operational amplifiers provide both low voltage noise and low current noise. This provides optimum noise performance over a wide range of sources, including reactive source impedances; refer to Figure 6. Above 2-kΩ source resistance, the operational amplifier contributes little additional noise; the voltage and current terms in the total noise equation become insignificant and the source resistance term dominates. Below 2 kΩ, operational amplifier voltage noise dominates over the resistor noise, but compares favorably with other audio operational amplifiers such as the OP176.

Copyright © 1997–2015, Texas Instruments Incorporated

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA134 series operational amplifiers are unity-gain stable, and suitable for a wide range of audio and general-purpose applications. All circuitry is independent in the dual version, assuring normal behavior when one amplifier in a package is overdriven or short-circuited. Power supply pins should be bypassed with 10-nF ceramic capacitors or larger to minimize power supply noise.

8.1.1 Operating Voltage

The OPA134 series of operational amplifiers operate with power supplies from ±2.5 V to ±18 V with excellent performance. Although specifications are production tested with ±15-V supplies, most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in *Typical Characteristics*.

8.1.2 Offset Voltage Trim

Offset voltage of OPA134 series amplifiers is laser-trimmed, and usually requires no user adjustment. The OPA134 (single operational amplifier version) provides offset trim connections on pins 1 and 8, identical to 5534 amplifiers. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 29. This adjustment should be used only to null the offset of the operational amplifier, not to adjust system offset or offset produced by the signal source. Nulling offset could change the offset voltage drift behavior of the operational amplifier. While it is not possible to predict the exact change in drift, the effect is usually small.

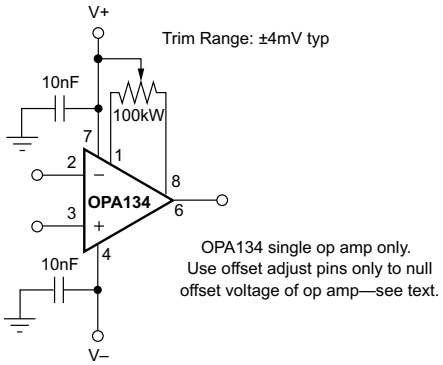


Figure 29. OPA134 Offset Voltage Trim Circuit

8.2 Typical Application

The OPAx134 family offers outstanding dc precision and AC performance. These devices operate up to 36-V supply rails and offer ultralow distortion and noise, as well as 8-MHz bandwidth and high capacitive load drive. These features make the OPAx134 a robust, high-performance operational amplifier for high-voltage professional audio applications.

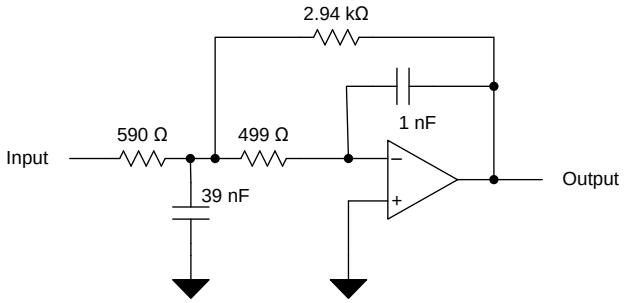


Figure 30. OPA134 2nd Order 30-kHz, Low Pass Filter Schematic

8.2.1 Design Requirements

- Gain = 5 V/V (inverting)
- Low pass cutoff frequency = 30 kHz
- –40 db/dec filter response
- Maintain less than 3-dB gain peaking in the gain versus frequency response

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 30. The voltage transfer function is:

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (2)$$

This circuit produces a signal inversion. For this circuit the gain at DC and the low pass cutoff frequency are calculated using Equation 3.

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (3)$$

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

Copyright © 1997–2015, Texas Instruments Incorporated

Typical Application (continued)

8.2.3 Application Curve

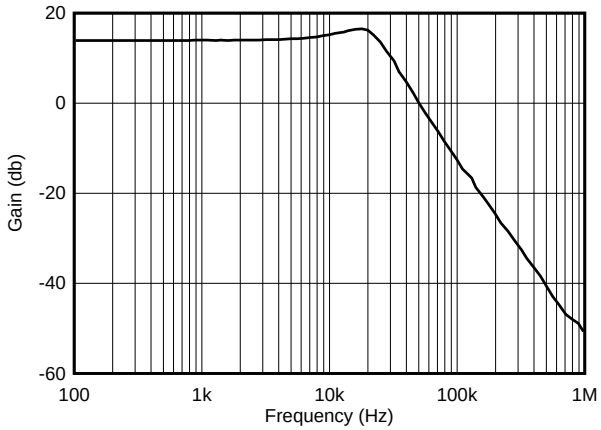


Figure 31. OPA134 2nd Order 30-kHz, Low Pass Filter Response

Copyright © 1997–2015, Texas Instruments Incorporated

9 Power Supply Recommendations

The OPAx134 is specified for operation from 5 V to 36 V (±2.5 V to ±18 V); many specifications apply from –40°C to 85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 36 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 10-nF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines*.

10 Layout

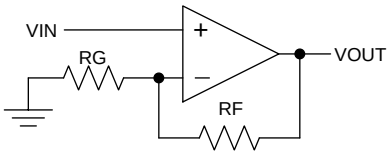
10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 10-nF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, SLOA089.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in *Layout Example*, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

Copyright © 1997–2015, Texas Instruments Incorporated

10.2 Layout Example



(Schematic Representation)

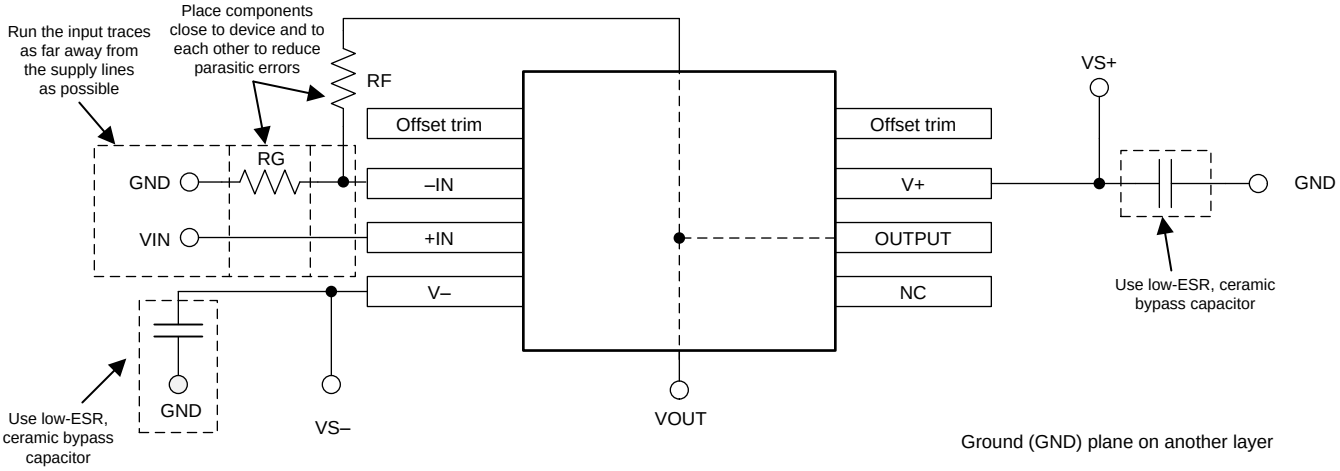


Figure 32. OPA134 Layout Example for the Noninverting Configuration

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 WEBENCH Filter Designer Tool

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

11.1.1.2 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.3 TI Precision Designs

The OPAx134 is featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *EMI Rejection Ratio of Operational Amplifiers*, SBOA128
- *Circuit Board Layout Techniques*, SLOA089

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA134	Click here	Click here	Click here	Click here	Click here
OPA2134	Click here	Click here	Click here	Click here	Click here
OPA4134	Click here	Click here	Click here	Click here	Click here

Copyright © 1997–2015, Texas Instruments Incorporated

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

SoundPlus, TINA-TI, E2E are trademarks of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 1997–2015, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA134PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA134PA	Samples
OPA134PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA134PA	Samples
OPA134UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 134UA	Samples
OPA134UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 134UA	Samples
OPA134UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 134UA	Samples
OPA134UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 134UA	Samples
OPA134UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 134UA	Samples
OPA2134PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA2134PA	Samples
OPA2134PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA2134PA	Samples
OPA2134UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2134UA	Samples
OPA2134UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2134UA	Samples
OPA2134UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2134UA	Samples
OPA2134UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2134UA	Samples
OPA2134UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2134UA	Samples
OPA4134UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4134UA	Samples
OPA4134UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4134UA	Samples
OPA4134UA/2K5E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4134UA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4134UAE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4134UA	Samples
SN412008DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2134UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

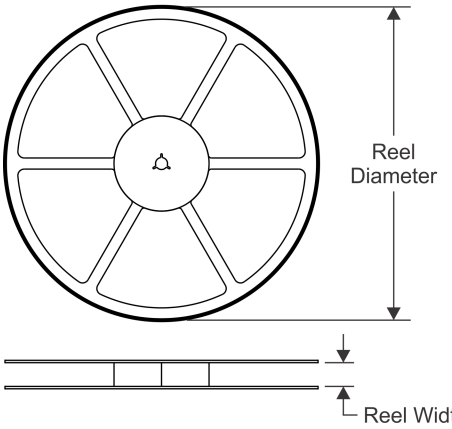
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

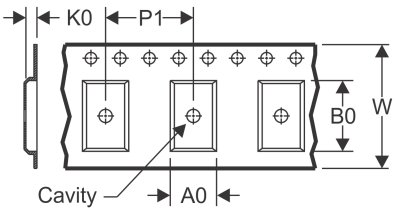
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

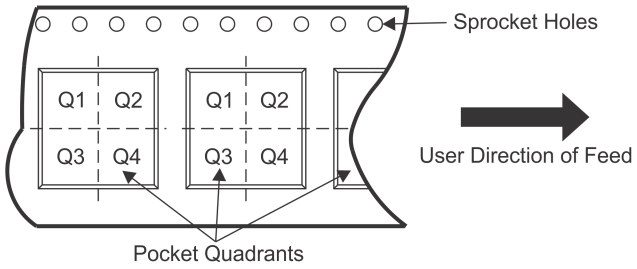


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

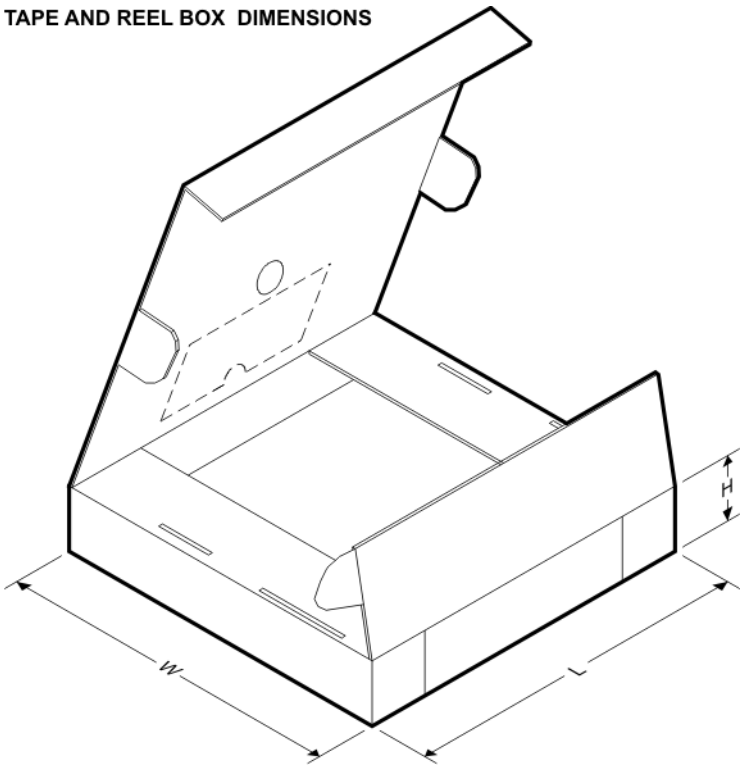
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA134UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2134UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4134UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

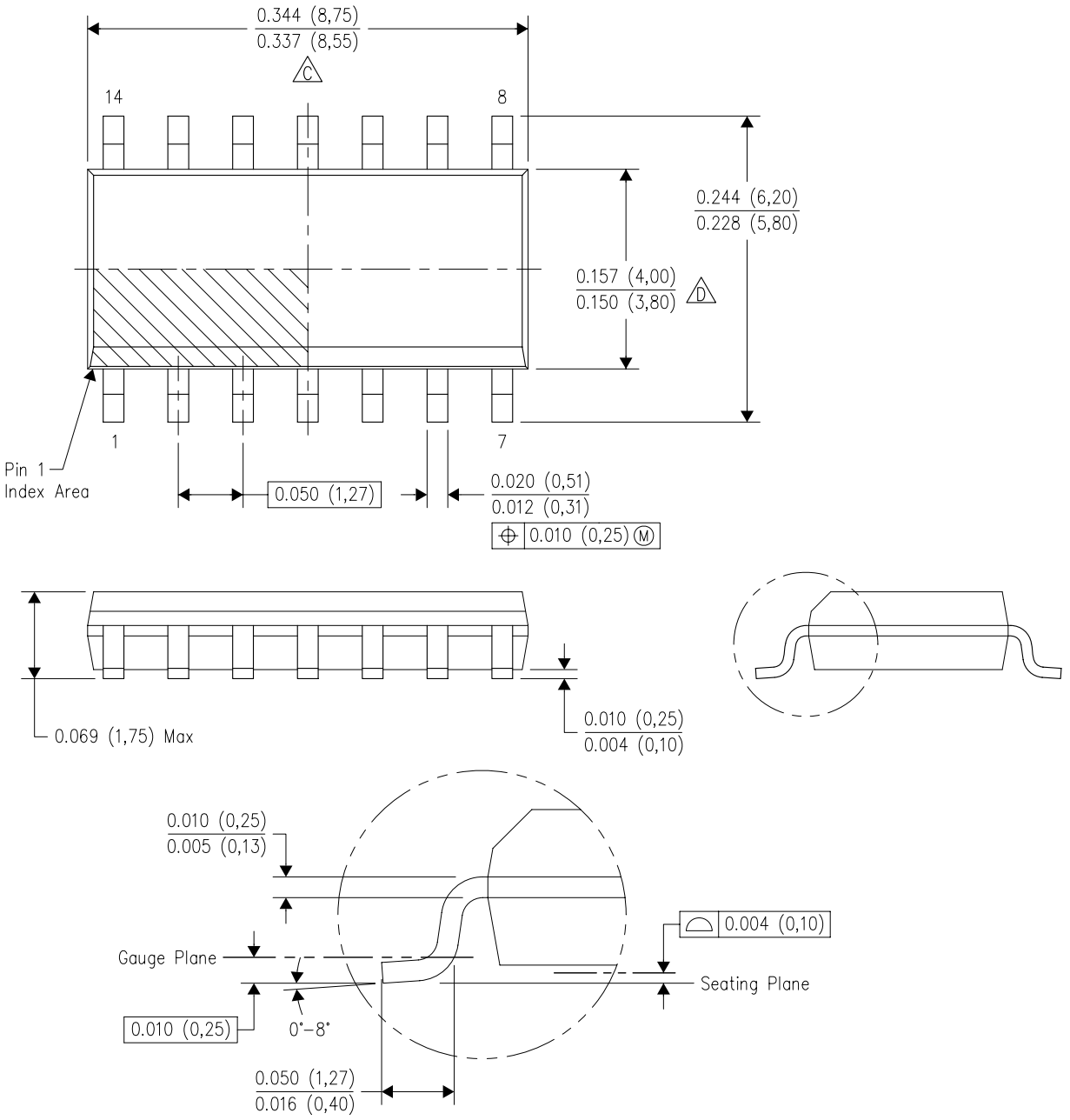
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA134UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA2134UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA4134UA/2K5	SOIC	D	14	2500	367.0	367.0	38.0

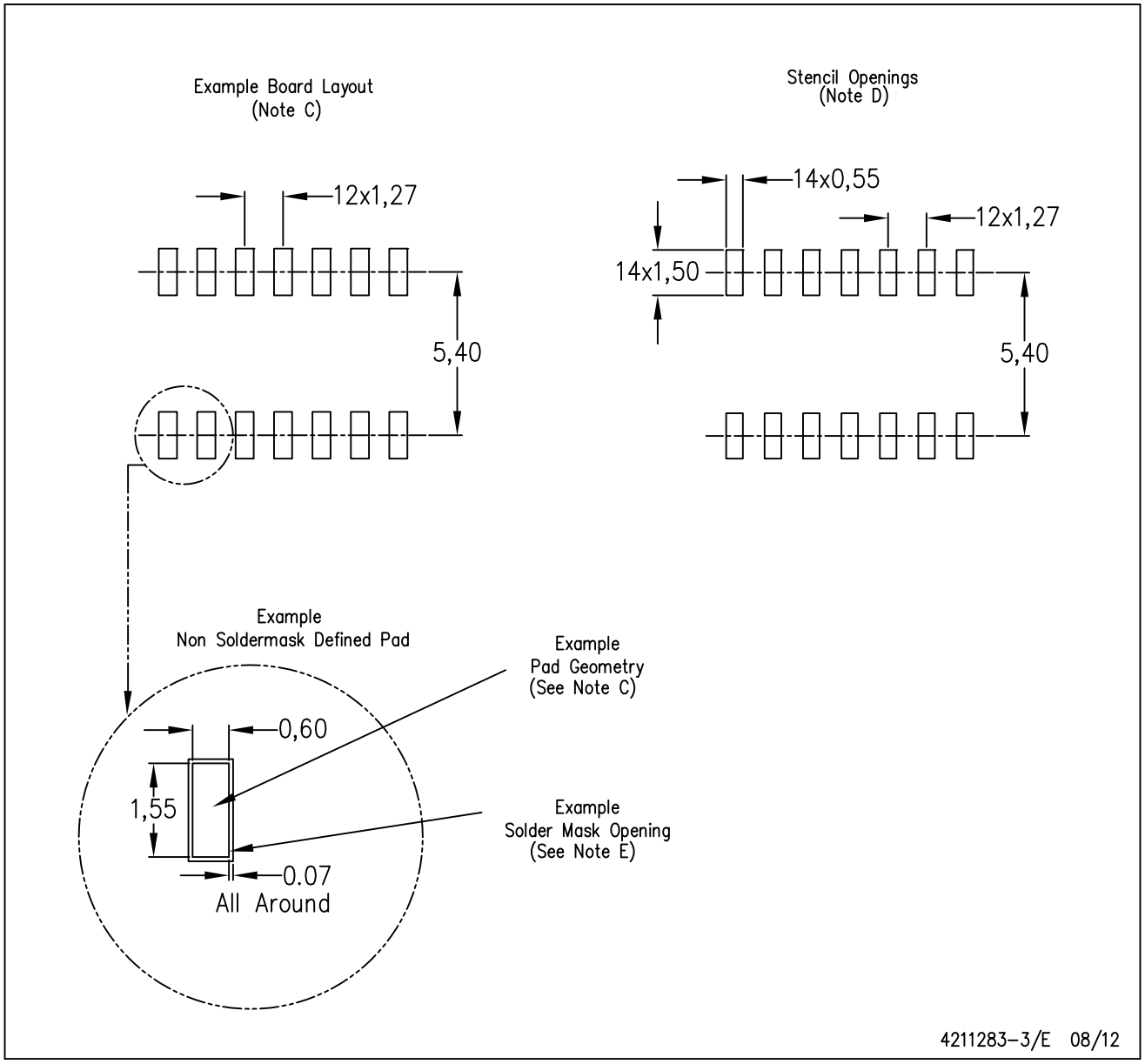
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

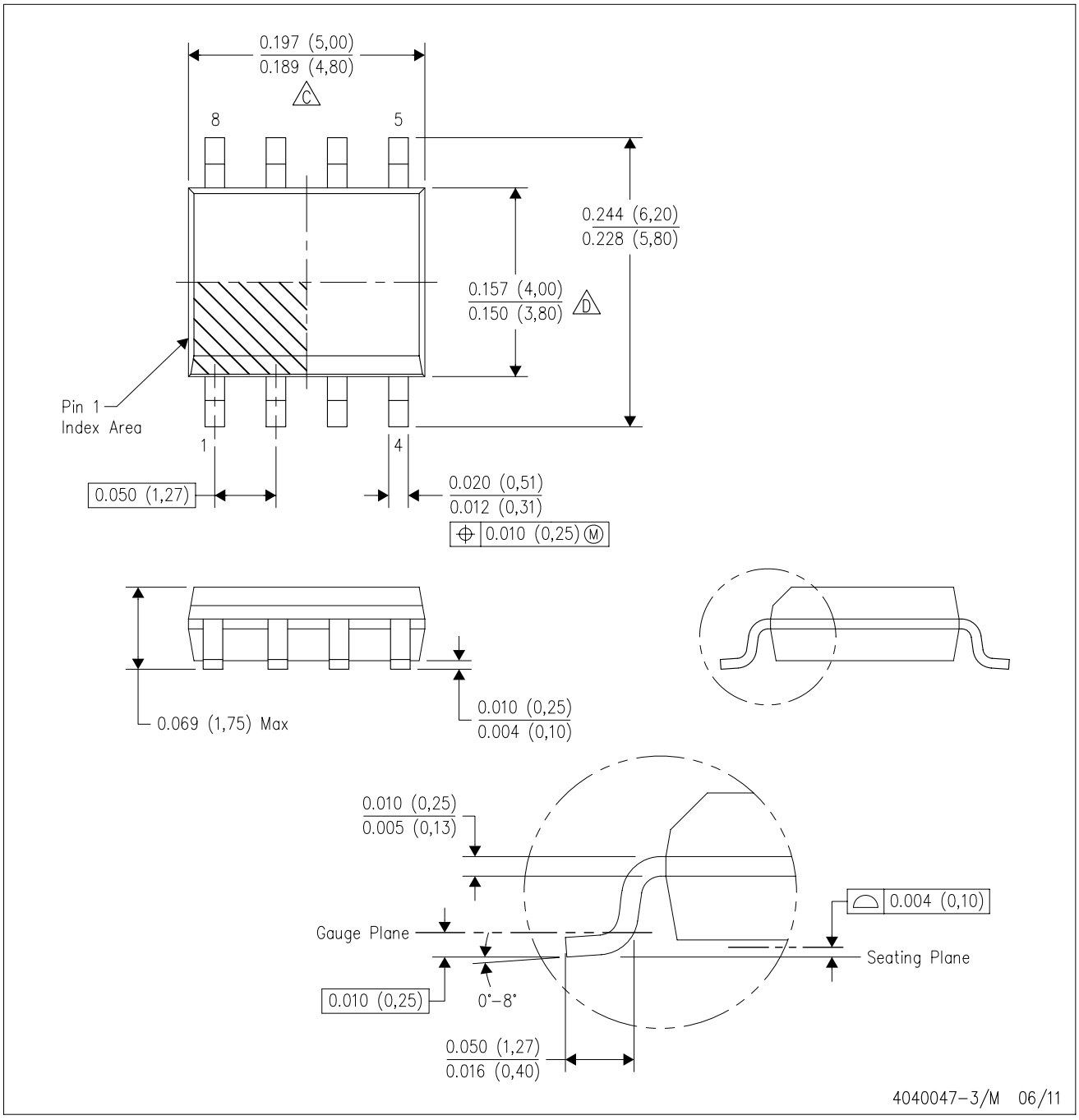
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



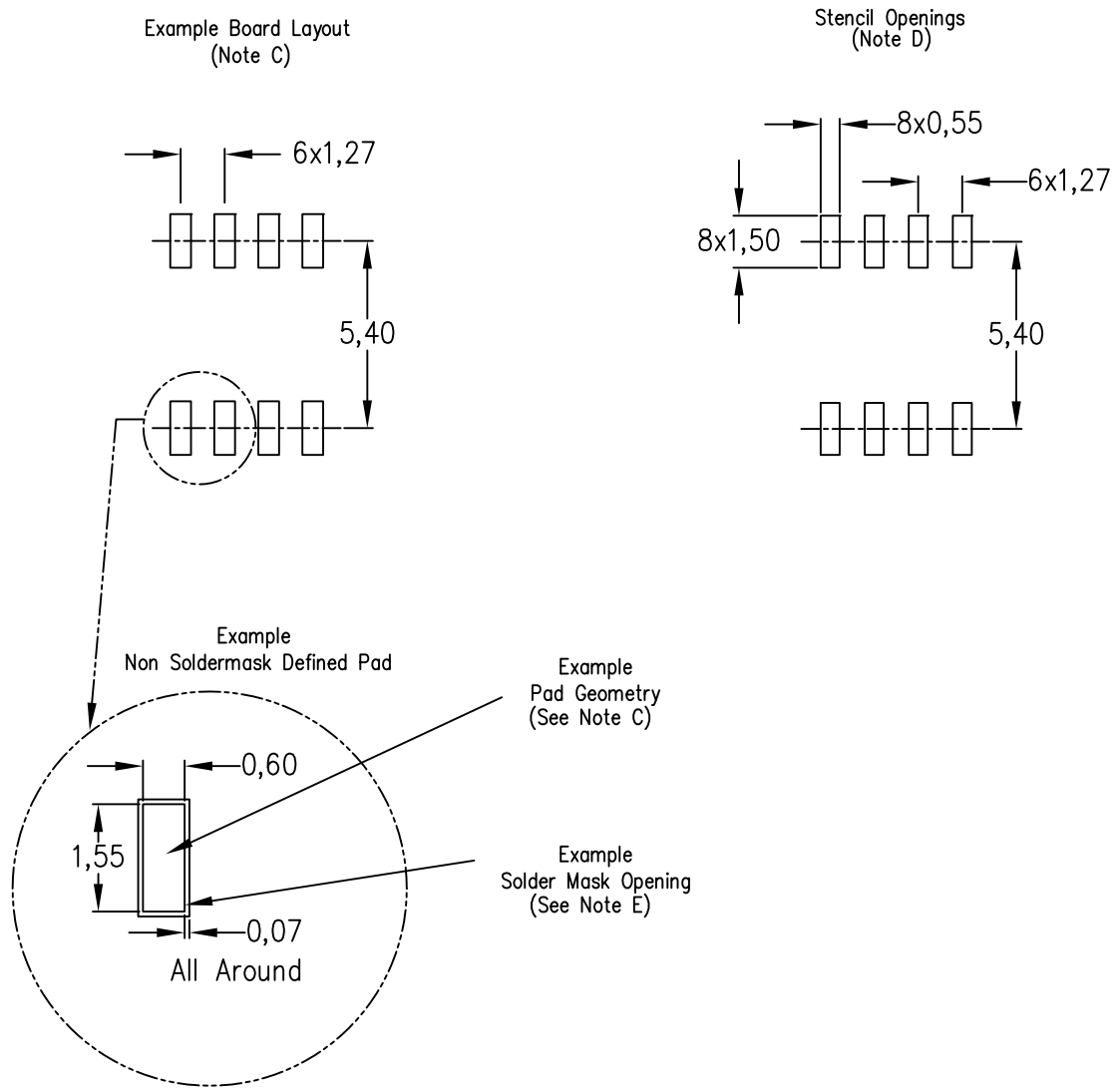
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



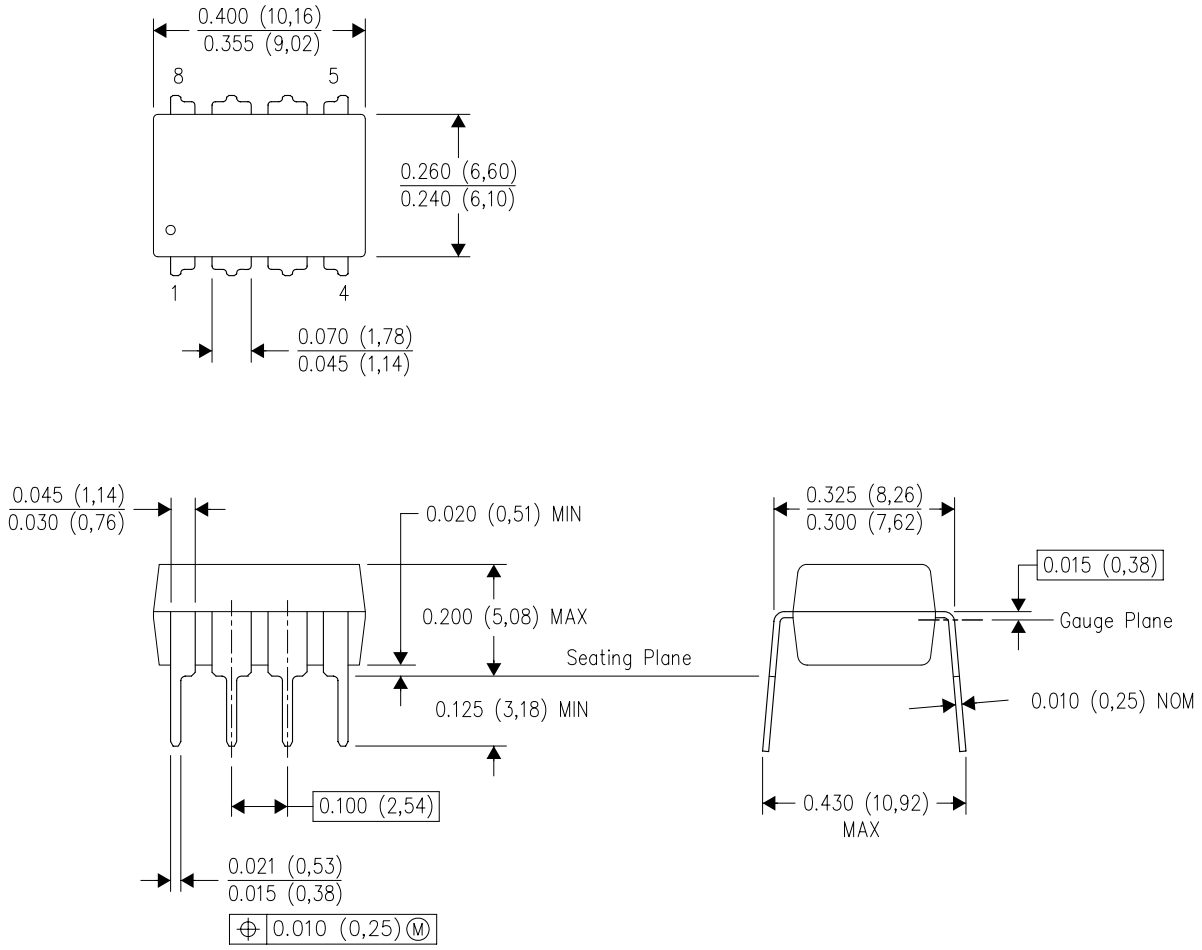
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.