Programmable Precision References

TL431, A, B Series

PROGRAMMABLE PRECISION REFERENCES

SEMICONDUCTOR TECHNICAL DATA

The TL431, A, B integrated circuits are three–terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from V_{ref} to 36 V with two external resistors. These devices exhibit a wide operating current range of 1.0 mA to 100 mA with a typical dynamic impedance of 0.22 Ω. The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 V reference makes it convenient to obtain a stable reference from 5.0 V logic supplies, and since the TL431, A, B operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

- Programmable Output Voltage to 36 V

- Voltage Reference Tolerance: ±0.4%, Typ @ 25°C (TL431B)

- Low Dynamic Output Impedance, 0.22 Ω Typical

- Sink Current Capability of 1.0 mA to 100 mA

- Equivalent Full–Range Temperature Coefficient of 50 ppm/°C Typical

- Temperature Compensated for Operation over Full Rated Operating Temperature Range
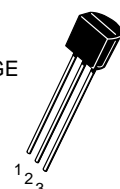
- Low Output Noise Voltage

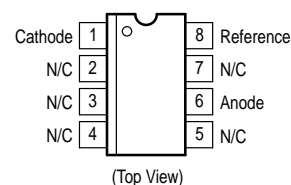**LP SUFFIX**
PLASTIC PACKAGE
CASE 29
(TO–92)

Pin 1. Reference
2. Anode
3. Cathode
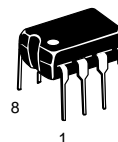
P SUFFIX
PLASTIC PACKAGE
CASE 626

DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro–8)

Cathode	1			8	Reference
N/C	2			7	N/C
N/C	3			6	Anode
N/C	4			5	N/C

(Top View)

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)

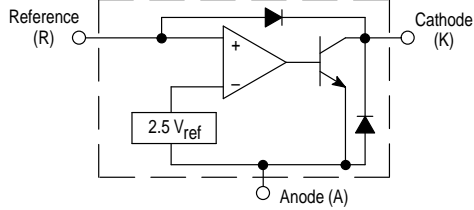| Cathode	1			8	Reference
Anode	2			7	Anode
	3			6	
N/C	4			5	N/C

(Top View)
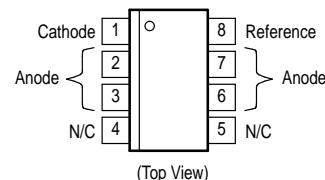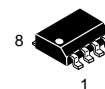
SOP–8 is an internally modified SO–8 package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases power dissipation capability when appropriately mounted on a printed circuit board. SOP–8 conforms to all external dimensions of the standard SO–8 package.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
TL431CLP, ACLP, BCLP		TO–92
TL431CP, ACP, BCP		Plastic
TL431CDM, ACDM, BCDM	$T_A = 0°$ to +70°C	Micro–8
TL431CD, ACD, BCD		SOP–8
TL431ILP, AILP, BILP		TO–92
TL431IP, AIP, BIP		Plastic
TL431IDM, AIDM, BIDM	$T_A = -40°$ to +85°C	Micro–8
TL431ID, AID, BID		SOP–8

Symbol

Representative Schematic Diagram

Component values are nominal

Representative Block Diagram
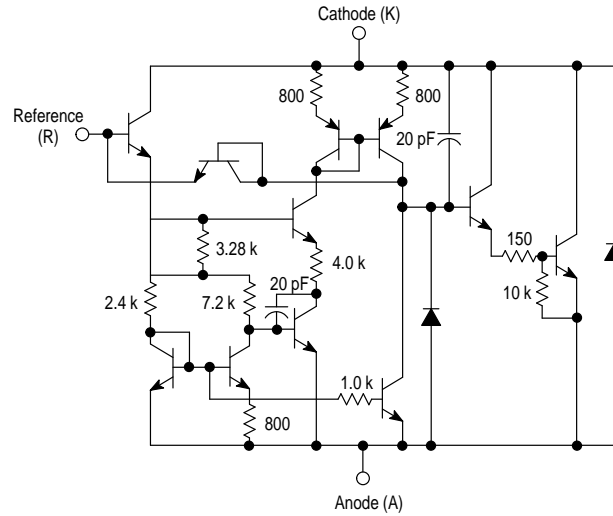
This device contains 12 active transistors.

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Cathode to Anode Voltage	V_{KA}	37	V
Cathode Current Range, Continuous	I_K	−100 to +150	mA
Reference Input Current Range, Continuous	I_{ref}	−0.05 to +10	mA
Operating Junction Temperature	T_J	150	°C

Operating Ambient Temperature Range
    TL431I, TL431AI, TL431BI
    TL431C, TL431AC, TL431BC
	T_A	
		−40 to +85
		0 to +70
			°C

Storage Temperature Range	T_{stg}	−65 to +150	°C

Total Power Dissipation @ T_A = 25°C
    Derate above 25°C Ambient Temperature
    D, LP Suffix Plastic Package
    P Suffix Plastic Package
    DM Suffix Plastic Package
	P_D	
		
		0.70
		1.10
		0.52
			W

Total Power Dissipation @ T_C = 25°C
    Derate above 25°C Case Temperature
    D, LP Suffix Plastic Package
    P Suffix Plastic Package
	P_D	
		
		1.5
		3.0
			W

NOTE: ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Min	Max	Unit
Cathode to Anode Voltage	V_{KA}	V_{ref}	36	V
Cathode Current	I_K	1.0	100	mA

THERMAL CHARACTERISTICS

Characteristic	Symbol	D, LP Suffix Package	P Suffix Package	DM Suffix Package	Unit
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	178	114	240	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	83	41	–	°C/W

TL431, A, B Series

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	TL431I			TL431C			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$, I_K = 10 mA T_A = 25°C $T_A = T_{low}$ to T_{high} (Note 1)	V_{ref}	 2.44 2.41	 2.495 –	 2.55 2.58	 2.44 2.423	 2.495 –	 2.55 2.567	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 1, 2) $V_{KA} = V_{ref}$, I_K = 10 mA	ΔV_{ref}	–	7.0	–	–	3.0	–	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I_K = 10 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref} ΔV_{KA} = 36 V to 10 V	$\dfrac{\Delta V_{ref}}{\Delta V_{KA}}$	 – –	 –1.4 –1.0	 –2.7 –2.0	 – –	 –1.4 –1.0	 –2.7 –2.0	mV/V
Reference Input Current (Figure 2) I_K = 10 mA, R1 = 10 k, R2 = ∞ T_A = 25°C $T_A = T_{low}$ to T_{high} (Note 1)	I_{ref}	 – –	 1.8 –	 4.0 6.5	 – –	 1.8 –	 4.0 5.2	μA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1, 4) I_K = 10 mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	–	0.8	2.5	–	0.4	1.2	μA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	–	0.5	1.0	–	0.5	1.0	mA
Off–State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	I_{off}	–	260	1000	–	2.6	1000	nA
Dynamic Impedance (Figure 1, Note 3) $V_{KA} = V_{ref}$, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	$\|Z_{KA}\|$	–	0.22	0.5	–	0.22	0.5	Ω

NOTES: 1. T_{low} = –40°C for TL431AIP TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431AIDM, TL431IDM, TL431BIDM
     = 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
     T_{high}= +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431IDM, TL431AIDM, TL431BIDM
     = +70°C for TL431ACP, TL431ACLP, TL431CP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
    2. The deviation parameter ΔV_{ref} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.

The average temperature coefficient of the reference input voltage, αV_{ref} is defined as:

$$V_{ref} \frac{ppm}{°C} = \frac{\left(\dfrac{\Delta V_{ref}}{V_{ref} \, @ \, 25°C}\right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A \, (V_{ref} \, @ \, 25°C)}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6.)

    Example : ΔV_{ref} = 8.0 mV and slope is positive,

      V_{ref} @ 25°C = 2.495 V, ΔT_A = 70°C $\alpha \, V_{ref} = \dfrac{0.008 \times 10^6}{70 \, (2.495)}$ = 45.8 ppm/°C

3. The dynamic impedance Z_{KA} is defined as $|Z_{KA}| = \dfrac{\Delta V_{KA}}{\Delta I_K}$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:
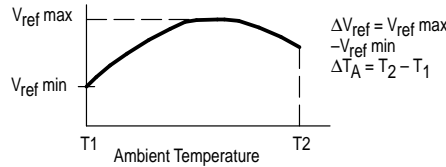
$$|Z_{KA}'| \approx |Z_{KA}| \left(1 + \frac{R1}{R2}\right)$$

TL431, A, B Series

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	TL431AI Min	TL431AI Typ	TL431AI Max	TL431AC Min	TL431AC Typ	TL431AC Max	TL431B Min	TL431B Typ	TL431B Max	Unit
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$, I_K = 10 mA T_A = 25°C $T_A = T_{low}$ to T_{high}	V_{ref}	 2.47 2.44	 2.495 –	 2.52 2.55	 2.47 2.453	 2.495 –	 2.52 2.537	 2.483 2.475	 2.495 2.495	 2.507 2.515	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 1, 2) $V_{KA} = V_{ref}$, I_K = 10 mA	ΔV_{ref}	–	7.0	–	–	3.0	–	–	3.0	–	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I_K = 10 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref} ΔV_{KA} = 36 V to 10 V	$\dfrac{\Delta V_{ref}}{\Delta V_{KA}}$	 – –	 –1.4 –1.0	 –2.7 –2.0	 – –	 –1.4 –1.0	 –2.7 –2.0	 – –	 –1.4 –1.0	 –2.7 –2.0	mV/V
Reference Input Current (Figure 2) I_K = 10 mA, R1 = 10 k, R2 = ∞ T_A = 25°C $T_A = T_{low}$ to T_{high} (Note 1)	ΔI_{ref}	 – –	 1.8 –	 4.0 6.5	 – –	 1.8 –	 4.0 5.2	 – –	 1.1 –	 2.0 4.0	µA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1) I_K = 10 mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	–	0.8	2.5	–	0.4	1.2	–	0.4	1.2	µA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	–	0.5	1.0	–	0.5	1.0	–	0.5	1.0	mA
Off–State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	I_{off}	–	260	1000	–	260	1000	–	230	500	nA
Dynamic Impedance (Figure 1, Note 3) $V_{KA} = V_{ref}$, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	$|Z_{KA}|$	–	0.22	0.5	–	0.22	0.5	–	0.14	0.3	Ω

NOTES: 1. T_{low} = –40°C for TL431AIP TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431AIDM, TL431IDM, TL431BIDM
= 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM

T_{high} = +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431IDM, TL431AIDM, TL431BIDM
= +70°C for TL431ACP, TL431ACLP, TL431CP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM

2. The deviation parameter ΔV_{ref} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.

$\Delta V_{ref} = V_{ref}$ max $-V_{ref}$ min
$\Delta T_A = T_2 - T_1$

The average temperature coefficient of the reference input voltage, αV_{ref} is defined as:

$$V_{ref}\,\frac{ppm}{°C} = \frac{\left(\dfrac{\Delta V_{ref}}{V_{ref}\,@\,25°C}\right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A\,(V_{ref}\,@\,25°C)}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example : ΔV_{ref} = 8.0 mV and slope is positive,

$V_{ref}\,@\,25°C = 2.495$ V, $\Delta T_A = 70°C$ $\alpha\,V_{ref} = \dfrac{0.008 \times 10^6}{70\,(2.495)} = 45.8$ ppm/°C

3. The dynamic impedance Z_{KA} is defined as $|Z_{KA}| = \dfrac{\Delta V_{KA}}{\Delta I_K}$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

$$|Z_{KA}'| \approx |Z_{KA}|\left(1 + \frac{R1}{R2}\right)$$

TL431, A, B Series
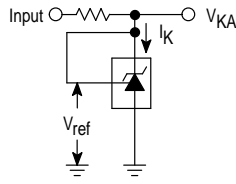
Figure 1. Test Circuit for $V_{KA} = V_{ref}$

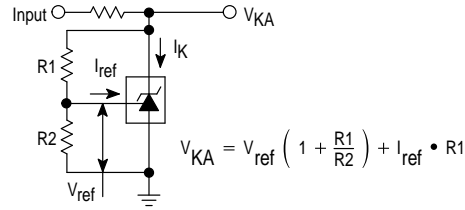**Figure 2. Test Circuit for $V_{KA} > V_{ref}$**

$$V_{KA} = V_{ref} \left(1 + \frac{R1}{R2} \right) + I_{ref} \cdot R1$$
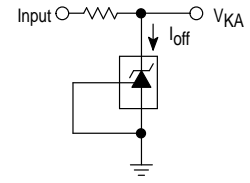
Figure 3. Test Circuit for I_{off}

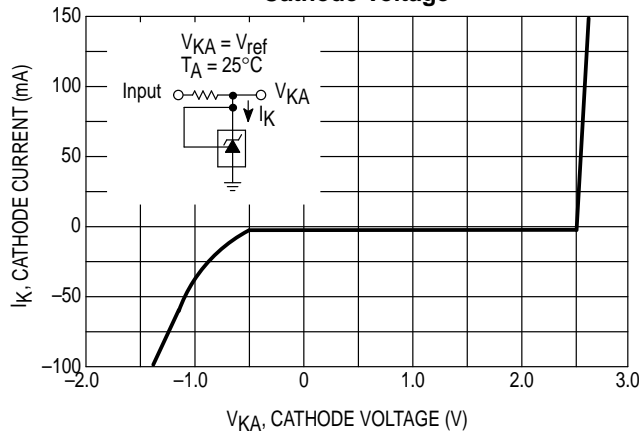**Figure 4. Cathode Current versus Cathode Voltage**

Figure 5. Cathode Current versus Cathode Voltage
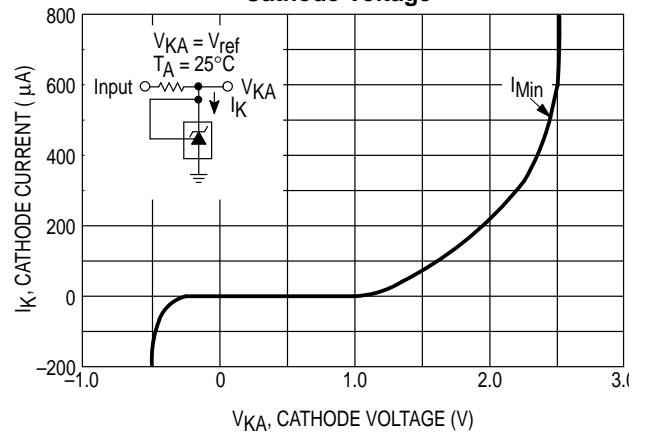

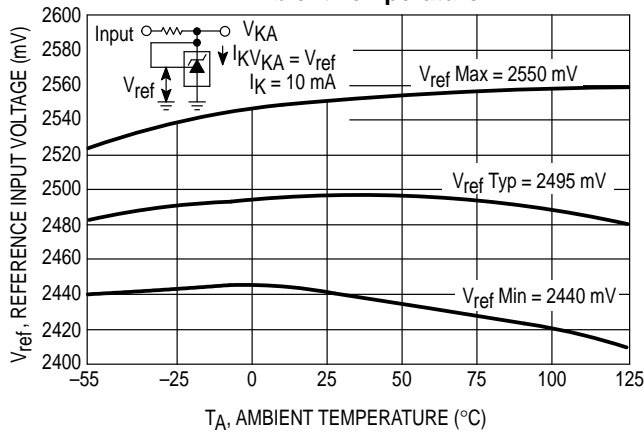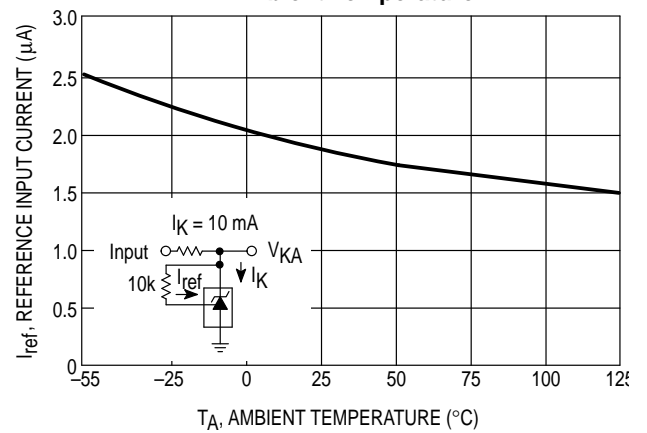**Figure 6. Reference Input Voltage versus Ambient Temperature**

Figure 7. Reference Input Current versus Ambient Temperature

**Figure 8. Change in Reference Input
Voltage versus Cathode Voltage**

$I_K = 10$ mA
$T_A = 25°C$

ΔV_{ref}, REFERENCE INPUT VOLTAGE (mV)

V_{KA}, CATHODE VOLTAGE (V)
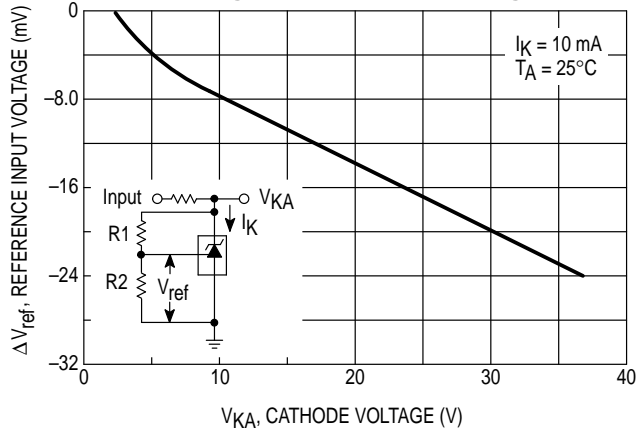
**Figure 9. Off–State Cathode Current
versus Ambient Temperature**

$V_{KA} = 36$ V
$V_{ref} = 0$ V

I_{off}, OFF–STATE CATHODE CURRENT (nA)

T_A, AMBIENT TEMPERATURE (5C)
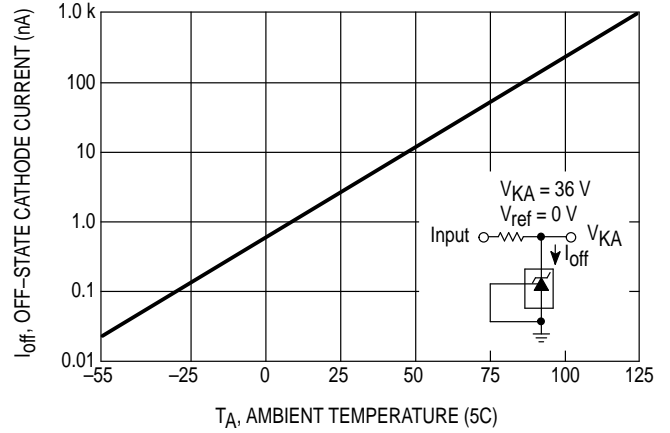
**Figure 10. Dynamic Impedance
versus Frequency**

$T_A = 25°C$
$\Delta I_K = 1.0$ mA to 100 mA

$|Z_{KA}|$, DYNAMIC IMPEDANCE (Ω)
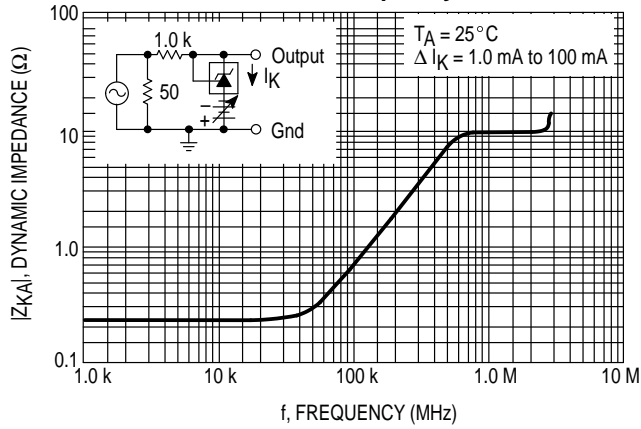
f, FREQUENCY (MHz)

**Figure 11. Dynamic Impedance
versus Ambient Temperature**

$V_{KA} = V_{ref}$
$\Delta I_K = 1.0$ mA to 100 mA
$f \leq 1.0$ kHz

$|Z_{KA}|$, DYNAMIC IMPEDANCE (Ω)

T_A, AMBIENT TEMPERATURE (°C)
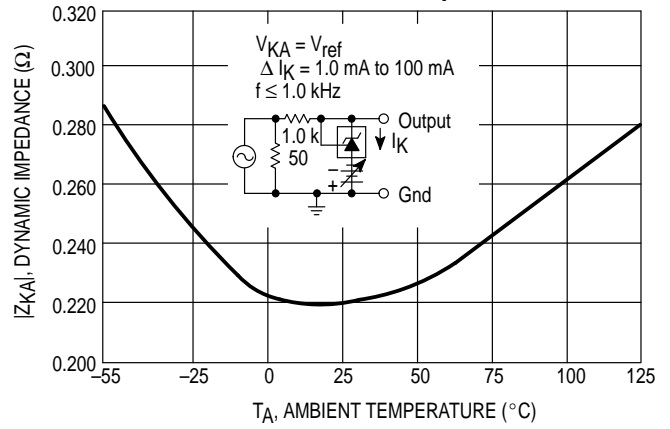
**Figure 12. Open–Loop Voltage Gain
versus Frequency**

$I_K = 10$ mA
$T_A = 25°C$

A_{VOL}, OPEN LOOP VOLTAGE GAIN (dB)

f, FREQUENCY (MHz)
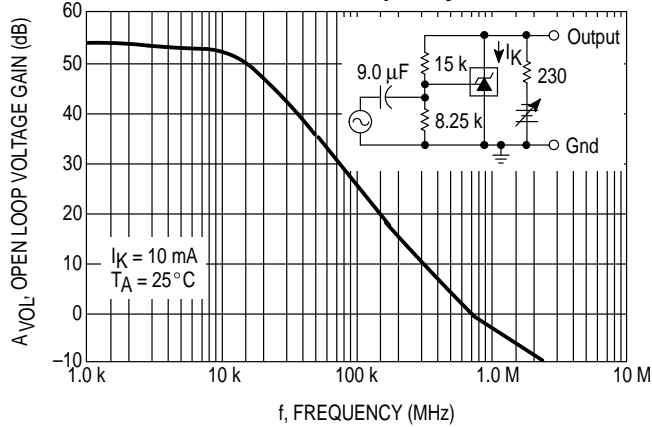
Figure 13. Spectral Noise Density

$V_{KA} = V_{ref}$
$I_K = 10$ mA
$T_A = 25°C$

NOISE VOLTAGE (nV/ $\sqrt{Hz}$)

f, FREQUENCY (Hz)
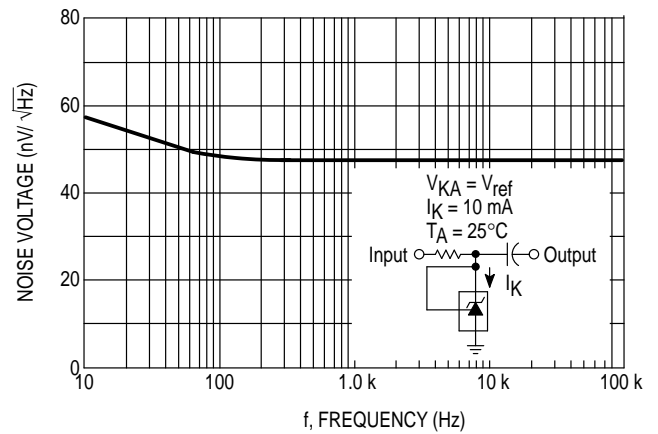
TL431, A, B Series

Figure 14. Pulse Response

Figure 15. Stability Boundary Conditions

A) $V_{KA} = V_{ref}$
B) $V_{KA} = 5.0$ V @ $I_K = 10$ mA
C) $V_{KA} = 10$ V @ $I_K = 10$ mA
D) $V_{KA} = 15$ V @ $I_K = 10$ mA
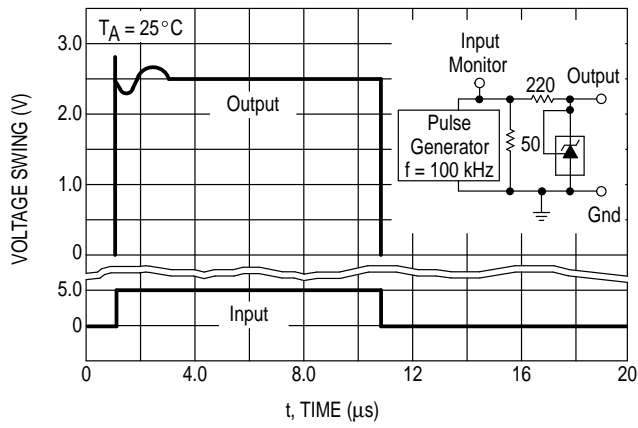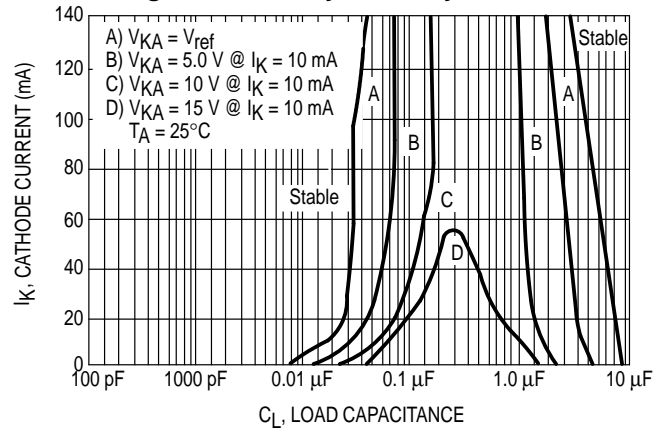$T_A = 25°C$

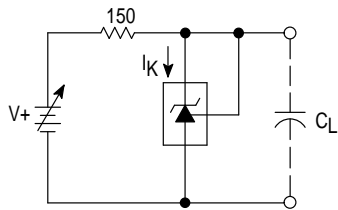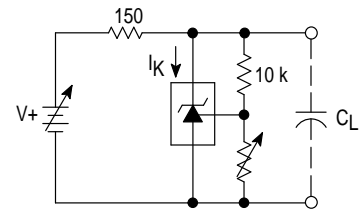### Figure 16. Test Circuit For Curve A of Stability Boundary Conditions

Figure 17. Test Circuit For Curves B, C, And D of Stability Boundary Conditions

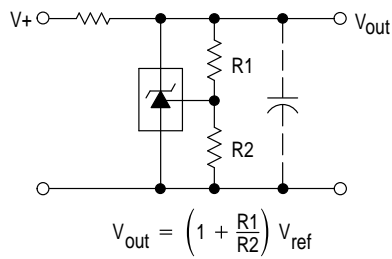## TYPICAL APPLICATIONS

Figure 18. Shunt Regulator

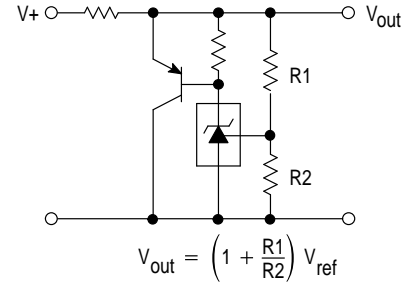$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

Figure 19. High Current Shunt Regulator

$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

TL431, A, B Series

**Figure 20. Output Control for a
Three–Terminal Fixed Regulator**

$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$V_{out}\ min = V_{ref} + 5.0V$$
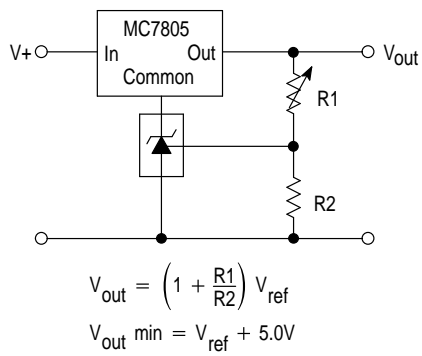
Figure 21. Series Pass Regulator

$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$V_{out}\ min = V_{ref} + V_{be}$$
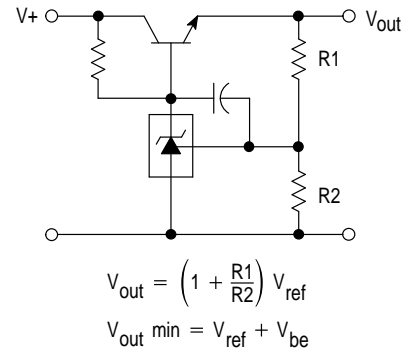
Figure 22. Constant Current Source

$$I_{out} = \frac{V_{ref}}{R_{CL}}$$
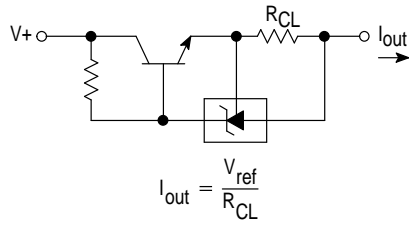
Figure 23. Constant Current Sink

$$I_{Sink} = \frac{V_{ref}}{R_S}$$
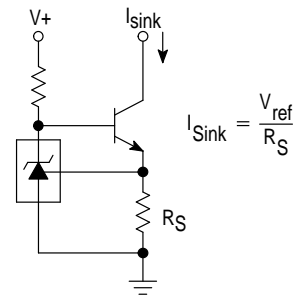
Figure 24. TRIAC Crowbar

$$V_{out(trip)} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$
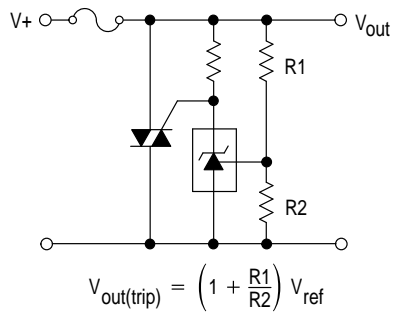
Figure 25. SRC Crowbar

$$V_{out(trip)} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$
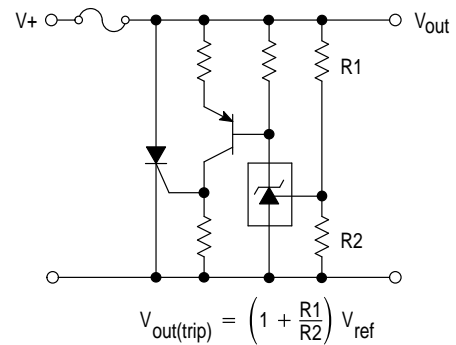
Figure 26. Voltage Monitor

L.E.D. indicator is 'on' when V+ is between the upper and lower limits.
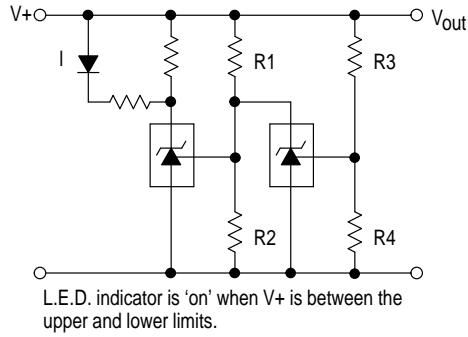
$$\text{Lower Limit} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$\text{Upper Limit} = \left(1 + \frac{R3}{R4}\right) V_{ref}$$

Figure 27. Single–Supply Comparator with Temperature–Compensated Threshold

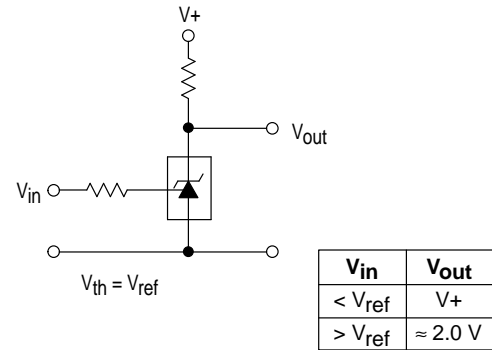$V_{th} = V_{ref}$

V_{in}	V_{out}
$< V_{ref}$	V+
$> V_{ref}$	≈ 2.0 V

Figure 28. Linear Ohmmeter

1N5305

25 V
2.0 mA

5.0 k 1%
50 k 1%
500 k 1%
5.0 M 1%

10 k Calibrate

$\frac{10\ k\Omega}{V}$

$\frac{100\ k\Omega}{V}$

$\frac{1.0\ k\Omega}{V}$

$\frac{1.0\ M\Omega}{V}$

25 V

LM11

Range

R_X

–5.0 V

V_{out}

$$R_x = V_{out} \cdot \frac{\Omega}{V}\ \text{Range}$$
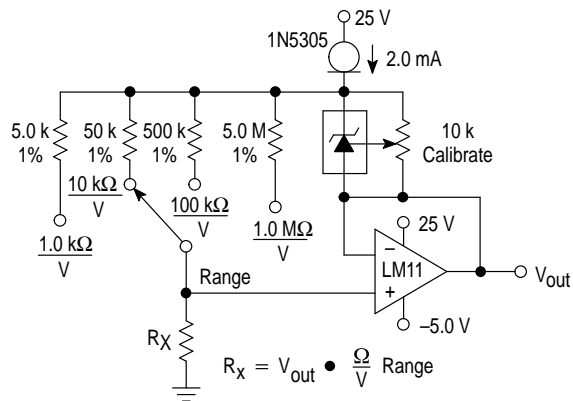
Figure 29. Simple 400 mW Phono Amplifier

38 V

330

$T_I = 330$ to $8.0\ \Omega$

$8.0\ \Omega$

T_I

360 k

+ 470 µF

1.0 µF

56 k

10 k

0.05 µF
Tone

25 k

Volume 47 k

* Thermalloy THM 6024 Heatsink on LP Package
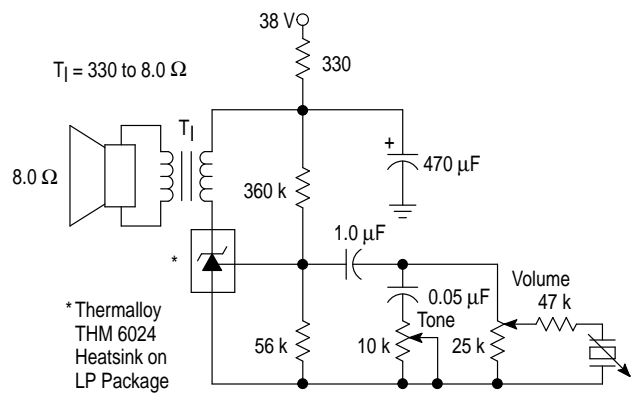
Figure 30. High Efficiency Step–Down Switching Converter
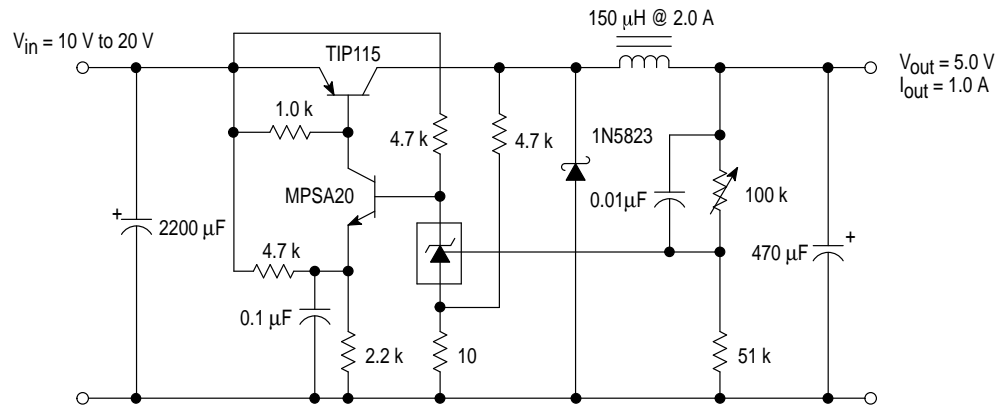
Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 20 V, I_O = 1.0 A	53 mV (1.1%)
Load Regulation	V_{in} = 15 V, I_O = 0 A to 1.0 A	25 mV (0.5%)
Output Ripple	V_{in} = 10 V, I_O = 1.0 A	50 mVpp P.A.R.D.
Output Ripple	V_{in} = 20 V, I_O = 1.0 A	100 mVpp P.A.R.D.
Efficiency	V_{in} = 15 V, I_O = 1.0 A	82%

APPLICATIONS INFORMATION

The TL431 is a programmable precision reference which is used in a variety of ways. It serves as a reference voltage in circuits where a non–standard reference voltage is needed. Other uses include feedback control for driving an optocoupler in power supplies, voltage monitor, constant current source, constant current sink and series pass regulator. In each of these applications, it is critical to maintain stability of the device at various operating currents and load capacitances. In some cases the circuit designer can estimate the stabilization capacitance from the stability boundary conditions curve provided in Figure 15. However, these typical curves only provide stability information at specific cathode voltages and at a specific load condition. Additional information is needed to determine the capacitance needed to optimize phase margin or allow for process variation.

A simplified model of the TL431 is shown in Figure 31. When tested for stability boundaries, the load resistance is 150 Ω. The model reference input consists of an input transistor and a dc emitter resistance connected to the device anode. A dependent current source, Gm, develops a current whose amplidute is determined by the difference between the 1.78 V internal reference voltage source and the input transistor emitter voltage. A portion of Gm flows through compensation capacitance, C_{P2}. The voltage across C_{P2} drives the output dependent current source, Go, which is connected across the device cathode and anode.

Model component values are:
V_{ref} = 1.78 V
Gm = 0.3 + 2.7 exp ($-I_C$/26 mA)
where I_C is the device cathode current and Gm is in mhos

Go = 1.25 ($V_{cp}2$) μmhos.

Resistor and capacitor typical values are shown on the model. Process tolerances are $\pm$20% for resistors, $\pm$10% for capacitors, and $\pm$40% for transconductances.

An examination of the device model reveals the location of circuit poles and zeroes:

$$P1 = \frac{1}{2\pi \ R_{GM} \ C_{P1}} = \frac{1}{2\pi * 1.0 \ M * 20 \ pF} = 7.96 \ kHz$$

$$P2 = \frac{1}{2\pi \ R_{P2} C_{P2}} = \frac{1}{2\pi * 10 \ M * 0.265 \ pF} = 60 \ kHz$$

$$Z1 = \frac{1}{2\pi \ R_{Z1} C_{P1}} = \frac{1}{2\pi * 15.9 \ k * 20 \ pF} = 500 \ kHz$$

In addition, there is an external circuit pole defined by the load:

$$P_L = \frac{1}{2\pi \ R_L C_L}$$

Also, the transfer dc voltage gain of the TL431 is:

$$G = G_M R_{GM} GoR_L$$

Example 1:

I_C = 10 mA, R_L = 230 Ω, C_L = 0. Define the transfer gain.

The DC gain is:

$$G = G_M R_{GM} GoR_L =$$
$$(2.138)(1.0 \ M)(1.25 \ \mu)(230) = 615 = 56 \ dB$$
$$Loop \ gain = G \ \frac{8.25 \ k}{8.25 \ k + 15 \ k} = 218 = 47 \ dB$$

The resulting transfer function Bode plot is shown in Figure 32. The asymptotic plot may be expressed as the following equation:

$$Av = 615 \ \frac{\left(1 + \dfrac{jf}{500 \ kHz}\right)}{\left(1 + \dfrac{jf}{8.0 \ kHz}\right)\left(1 + \dfrac{jf}{60 \ kHz}\right)}$$

The Bode plot shows a unity gain crossover frequency of approximately 600 kHz. The phase margin, calculated from the equation, would be 55.9 degrees. This model matches the Open–Loop Bode Plot of Figure 12. The total loop would have a unity gain frequency of about 300 kHz with a phase margin of about 44 degrees.
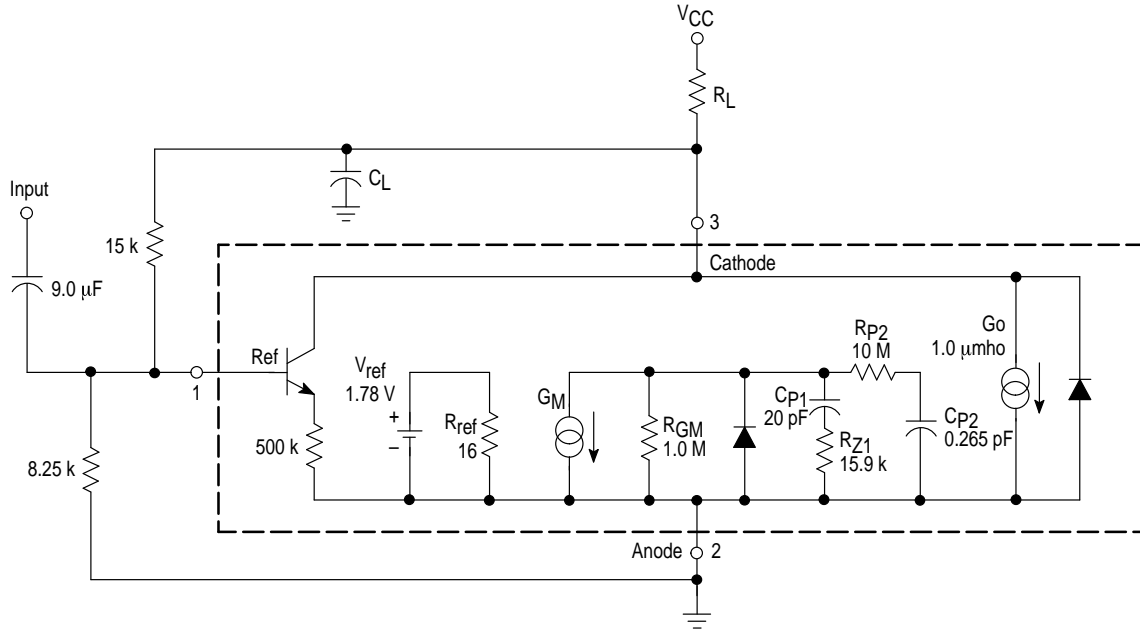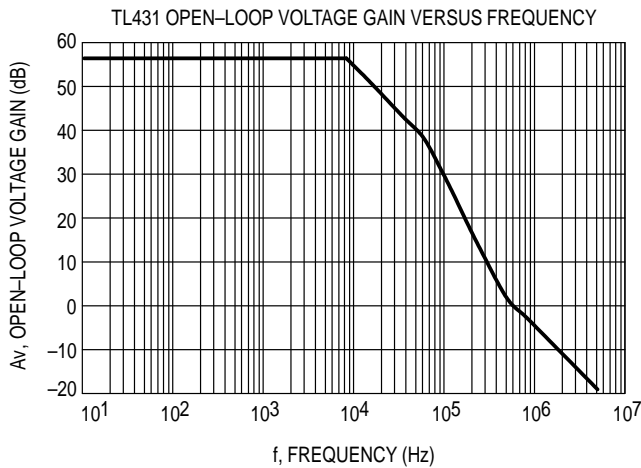
Figure 31. Simplified TL431 Device Model

**Figure 32. Example 1
Circuit Open Loop Gain Plot**

TL431 OPEN–LOOP VOLTAGE GAIN VERSUS FREQUENCY

Example 2.

I_C = 7.5 mA, R_L = 2.2 kΩ, C_L = 0.01 μF. Cathode tied to reference input pin. An examination of the data sheet stability boundary curve (Figure 15) shows that this value of load capacitance and cathode current is on the boundary. Define the transfer gain.

The DC gain is:

$$G = G_M R_{GM} G_O R_L =$$

$$(2.323)(1.0\ M)(1.25\ \mu)(2200) = 6389 = 76\ dB$$

The resulting open loop Bode plot is shown in Figure 33. The asymptotic plot may be expressed as the following equation:

$$Av = 615\ \frac{\left(1 + \dfrac{jf}{500\ kHz}\right)}{\left(1 + \dfrac{jf}{8.0\ kHz}\right)\left(1 + \dfrac{jf}{60\ kHz}\right)\left(1 + \dfrac{jf}{7.2\ kHz}\right)}$$

Note that the transfer function now has an extra pole formed by the load capacitance and load resistance.

Note that the crossover frequency in this case is about 250 kHz, having a phase margin of about −46 degrees. Therefore, instability of this circuit is likely.

**Figure 33. Example 2
Circuit Open Loop Gain Plot**

TL431 OPEN–LOOP BODE PLOT WITH LOAD CAP
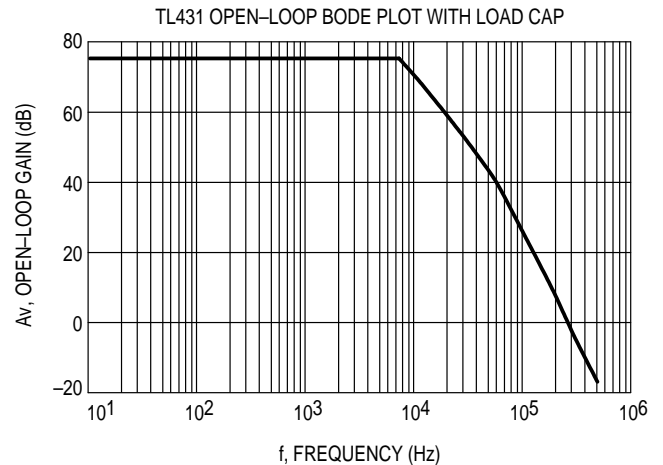
With three poles, this system is unstable. The only hope for stabilizing this circuit is to add a zero. However, that can only be done by adding a series resistance to the output capacitance, which will reduce its effectiveness as a noise filter. Therefore, practically, in reference voltage applications, the best solution appears to be to use a smaller value of capacitance in low noise applications or a very large value to provide noise filtering and a dominant pole rolloff of the system.

TL431, A, B Series

OUTLINE DIMENSIONS

**SECTION X–X**
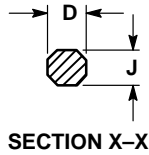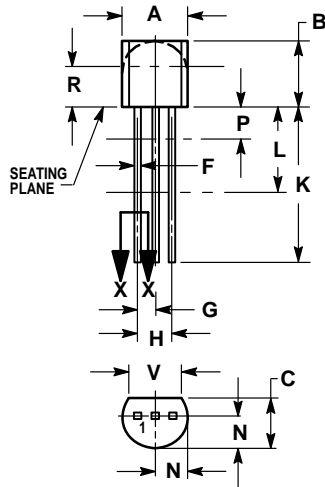
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—
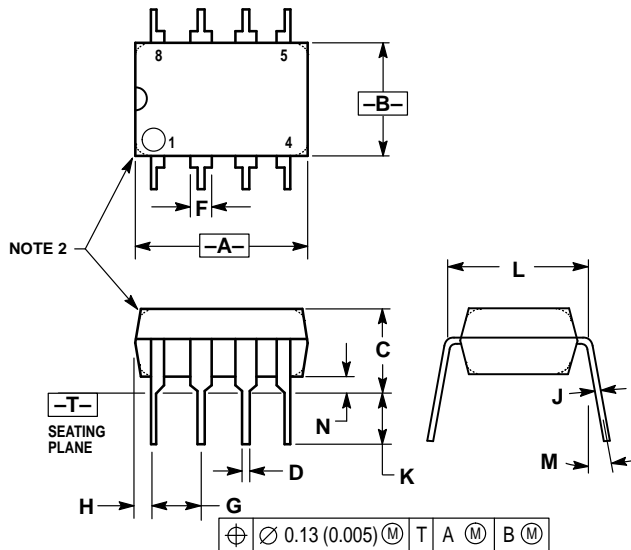
NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
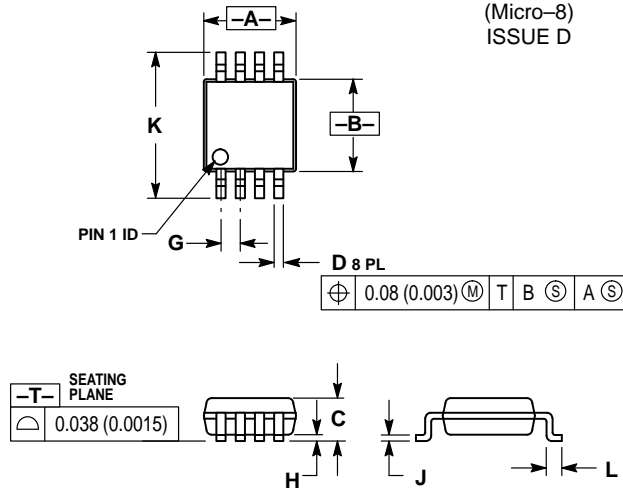3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

⊕ | ⌀ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ

TL431, A, B Series

OUTLINE DIMENSIONS

DM SUFFIX
PLASTIC PACKAGE
CASE 846A–02
(Micro–8)
ISSUE D

NOTES:
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
7. CONTROLLING DIMENSION: MILLIMETER.
8. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
9. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	—	1.10	—	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

⊕ | 0.08 (0.003) Ⓜ | T | B Ⓢ | A Ⓢ

SEATING PLANE
⌒ | 0.038 (0.0015)

PIN 1 ID

D SUFFIX
PLASTIC PACKAGE
CASE 751–06
(SOP–8)
ISSUE T
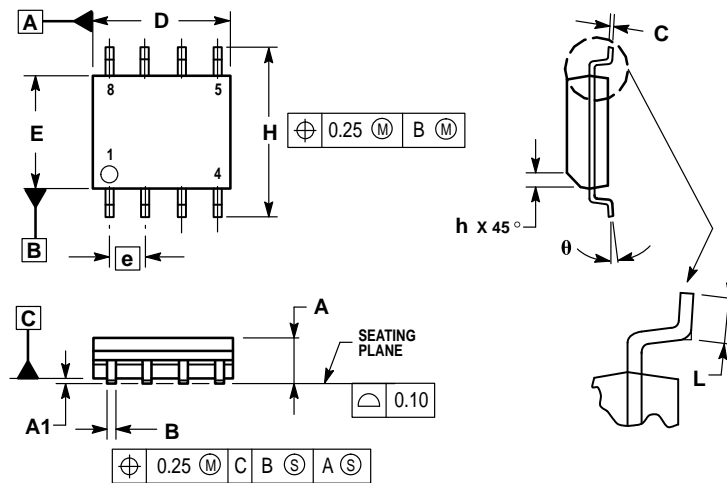
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

⊕ | 0.25 Ⓜ | B Ⓜ

SEATING PLANE
⌒ | 0.10

⊕ | 0.25 Ⓜ | C | B Ⓢ | A Ⓢ

h x 45°

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°